DATA SHEET

UCB1100
Advanced modem/audio analog front-end

Preliminary specification

1997 Apr 11

Philips
Semiconductors

PHILIPS

FEATURES

- 48 pin LQFP (SOT313) small body SMD package and low external component count results in minimal PCB space requirement
- 12-bit sigma delta audio codec with programmable sample rate, input and output voltage levels, capable of connecting directly to speaker and microphone, including digitally controlled mute, loopback and clip detection functions
- 14-bit sigma delta telecom codec with programmable sample rate, including digitally controlled input voltage level, mute, loopback and clip detection functions. The telecom codec can be directly connected to a Data Access Arrangement (DAA) and includes a built in sidetone suppression circuit
- Complete 4 wire resistive touch screen interface circuit supporting position, pressure and plate resistance measurements
- 10-bit successive approximation ADC with internal track and hold circuit and analog multiplexer for touch screen read-out and monitoring of four external high voltage (7.5V) analog voltages
- High speed, 4 wire serial interface data bus (SIB) for communication to the system controller
- 3.3V supply voltage and built in power saving modes make the UCB1100 optimal for portable and battery powered applications
- Maximum operating current 25 mA
- 10 general purpose IO pins

APPLICATIONS

- Handheld PCs (HPC)/Personal Intelligent Communicators (PIC)/ Personal Digital Assistants (PDA)
- Smart Mobile Phones
- Screen/Web Phones
- Internet Access Terminal
- Modems

GENERAL DESCRIPTION

The UCB1100 is a single chip, integrated mixed signal audio and telecom codec. The single channel audio codec is designed for direct connection of a microphone and a speaker. The built-in telecom codec can directly be connected to a DAA and supports high speed modem protocols. The incorporated analog to digital converter and the touch screen interface provides complete control and read-out of an 4 wire resistive touch screen. The 10 general purpose I/O pins provides programmable inputs and/or outputs to the system.

The UCB1100 has a serial interface bus (SIB) intended to communicate to the system controller. Both the codec input data and codec output data and the control register data are multiplexed on this SIB interface.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UCB1100HL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM

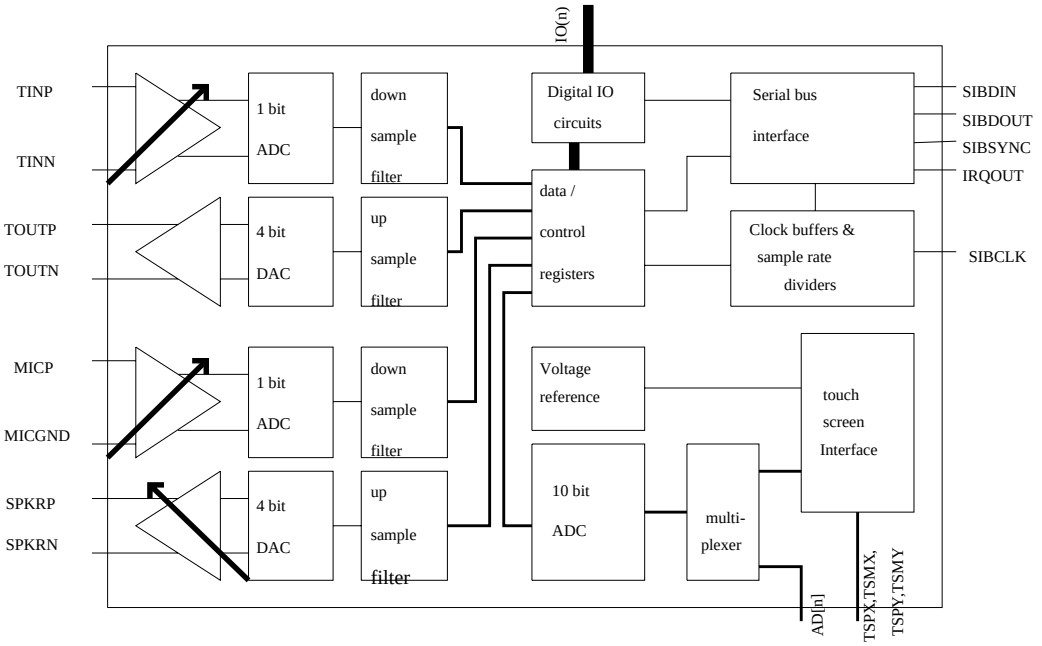


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	RESET STATE	TYPE[1]
IO7	1	general purpose I/O pins	input	I/O_C
IO8	2	general purpose I/O pins	input	I/O_C
IO9	3	general purpose I/O pins	input	I/O_C
ADCSYNC	4	ADC synchronization pulse input	–	I_C
V_{SSD}	5	digital ground	–	S[2]
n.c	6	not connected	–	–
V_{SSA2}	7	analog speaker driver ground	–	S
SKPRN	8	negative speaker output	hi Z	O_A
SPRKP	9	positive speaker output	hi Z	O_A
V_{DDA2}	10	analog speaker driver supply	–	S
TOUTP	11	positive telecom codec output	hi Z	O_A
TOUTN	12	negative telecom codec output	hi Z	O_A
TEST	13	test mode protection	‘0’	I_C
TINN	14	negative telecom codec input	hi Z	I_A
TINP	15	positive telecom codec input	hi Z	I_A
VREFBYP	16	external reference voltage input; external filter connection	hi Z	I/O_A
V_{DDA1}	17	analog supply	–	S
V_{SSA1}	18	analog ground	–	S
n.c	19	not connected	–	–
MICGND	20	microphone ground switch input	hi Z	I_A
MICP	21	microphone signal input	hi Z	I_A
AD3	22	analog voltage inputs	hi Z	I_A
AD2	23	analog voltage inputs	hi Z	I_A
AD1	24	analog voltage inputs	hi Z	I_A
AD0	25	analog voltage inputs	hi Z	I_A
V_{SSA3}	26	analog touch screen ground	–	S
TSPY	27	positive Y-plate touch screen	hi Z	I/O_A
TSMX	28	negative X-plate touch screen	hi Z	I/O_A
TSMY	29	negative Y-plate touch screen	hi Z	I/O_A
TSPX	30	positive X-plate touch screen	hi Z	I/O_A
n.c	31	not connected	–	–
V_{DDD}	32	digital supply	–	S
IO0	33	general purpose I/O pins	input	I/O_C
IO1	34	general purpose I/O pins	input	I/O_C
IO2	35	general purpose I/O pins	input	I/O_C
IO3	36	general purpose I/O pins	input	I/O_C
V_{SSD}	37	digital ground	–	S
$\overline{RESET}$	38	asynchronous reset input	–	I_C
SIBSYNC	39	SIB synchronization input	–	I_C

SYMBOL	PIN	DESCRIPTION	RESET STATE	TYPE(1)
SIBDOUT	40	SIB data output	'0'/hi Z	O_C
SIBCLK	41	SIB serial interface clock	–	I_C
SIBDIN	42	SIB data input	–	I_C
IRQOUT	43	interrupt output	'0'	O_C
n.c	44	not connected	–	–
IO4	45	general purpose I/O pins	input	I/O_C
IO5	46	general purpose I/O pins	input	I/O_C
IO6	47	general purpose I/O pins	input	I/O_C
V_{DDD}	48	digital supply	–	S

Notes

1. I/O_C = CMOS bidirectional; I_D = digital input; S = supply; O_A = analog output; I_C = CMOS input; I_A = analog input; I/O_A = analog bidirectional; O_C = CMOS output.
2. V_{SSD} (pins 5 and 37) and V_{SSA1} (pin 18) are connected internally within the UCB1100.
3. SKPRN/SPKRP (pins 8 and 9), TINN/TINP (pins 14 and 15) and TOUTP/TOUTN are differential pairs
4. TEST (pin 13) is connected to an internal pull-down resistor. This pin should be held LOW during normal operation of the UCB1100.
5. The not connected pins (pins 6, 19 31 and 44) are reserved for future applications and should be left floating.

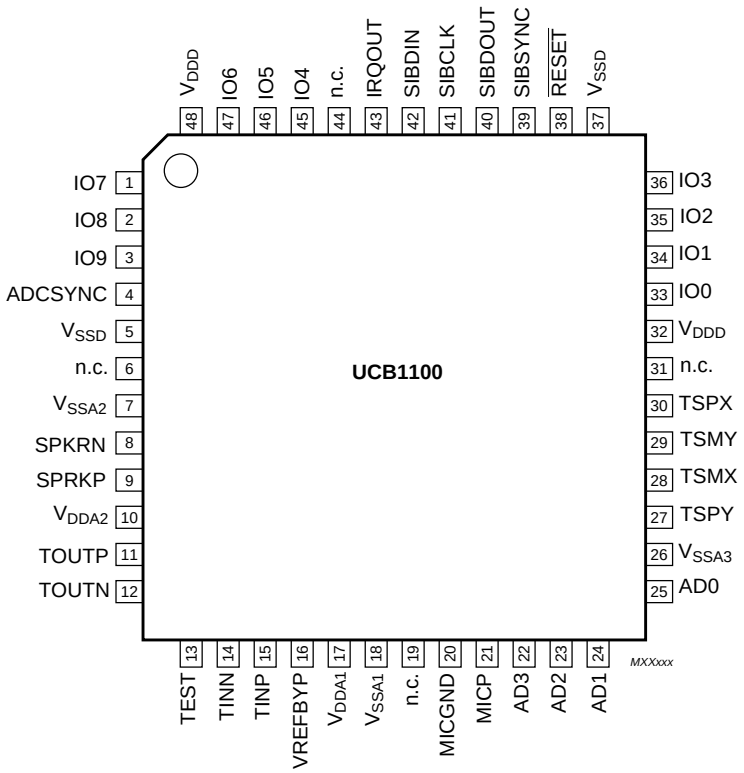


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The UCB1100 consists of several analog and digital sub circuits which can be programmed via the Serial Interface Bus (SIB). This enables the user to set the UCB1100 functionality according to actual application requirements.

AUDIO CODEC

The audio codec contains an input channel, built up with an 64 times oversampling sigma delta analog to digital converter (ADC) with digital decimation filters and a programmable gain microphone preamplifier. The programmable gain microphone amplifier features a built-in AC coupling stage, which reduces the distortion of this stage at high gain settings, caused by the offset voltages of the internal amplifiers. It can be deactivated for improved performance at low gain settings.

The output path consists of a digital up sample filter, a 64 time oversampling 4 bit digital to analog converter (DAC) circuit followed by a BTL speaker driver, capable of driving a 16 Ω speaker. The output path features a digital programmable attenuation and a mute function.

The audio codec also incorporates a loopback mode, in which codec output path and the input path are connected in series.

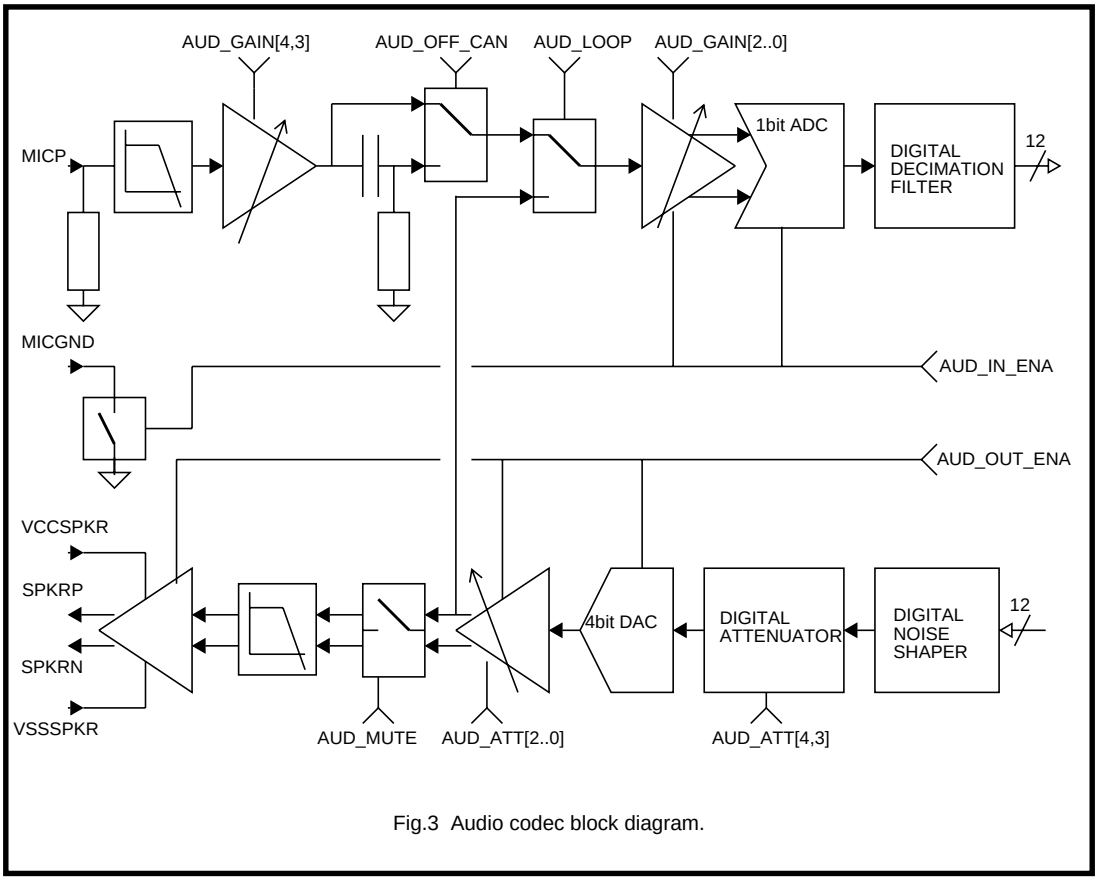


Fig.3 Audio codec block diagram.

The audio sample rate (f_{sa}) is derived from the SIB interface clock pin (SIBCLK) and is programmable through the SIB interface using AUD_DIV[n]. The audio sample rate is given by the following equation:

$$f_{sa} = \frac{(2 \times f_{SIBCLK})}{(64 \times AUD\_DIV[n])} \qquad (8 < AUD\_DIV[n] < 128)$$

For example, a serial clock of 9.216 MHz, with a divisor of 12, results in an audio sample rate of 24.0 kHz. Both the rising and the falling edges of SIBCLK are used in case AUD_DIV[n] is set to an odd number, which demands a 50% duty cycle of SIBCLK to obtain time equidistant sampling.

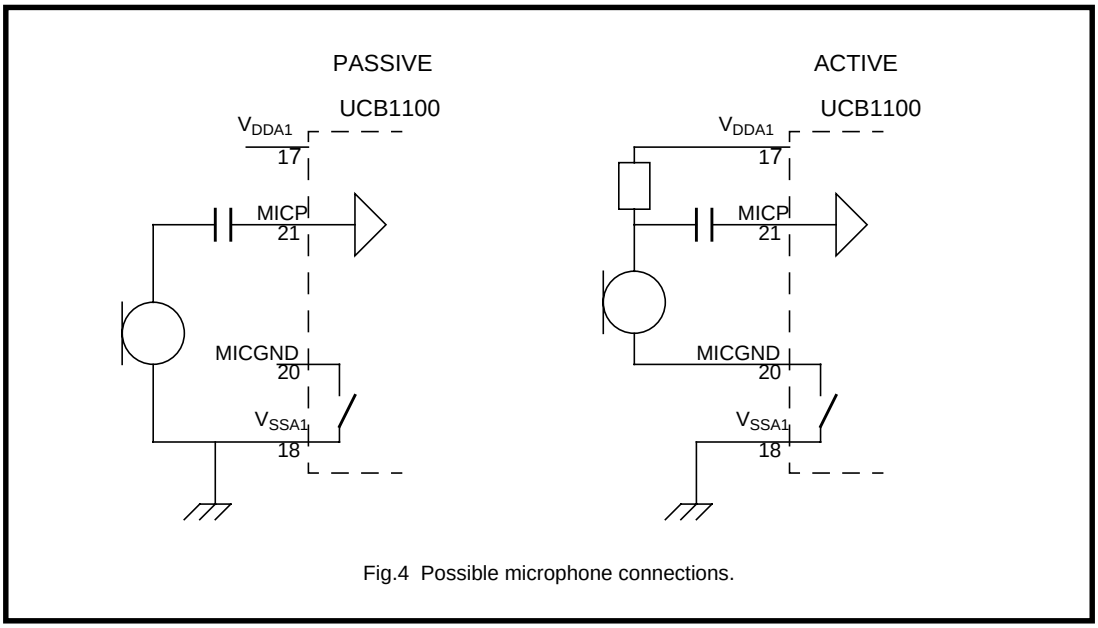


Fig.4 Possible microphone connections.

The UCB1100 audio codec input path accepts microphone signals directly, only a DC blocking capacitor is needed since the MICP input is biased around 1.4V. The 'ground' side of the microphone is either connected to the analog ground (V_{ssa1}) or to the MICGND pin. The latter will decrease the current consumption of active microphones, since the MICGND pin is made Hi-Z when the audio codec input path is disabled.

The full scale input voltage of the audio input path is programmable in 1.5 dB steps by setting the appropriate number in AUDIO_GAIN[n] in the audio control register A.

A clip detection circuit will inform the user whenever the input voltage exceeds the maximum input voltage, since this will lead to a high distortion. In that case AUD_CLIP_STAT in the audio control register B is set. When ACLIP_RIS_INT is set, an interrupt is generated on the IRQOUT pin on the rising edge of the clip detect signal. When ACLIP_FAL_INT is set, an interrupt is generated on the falling edge of the clip detect signal.

The frequency response of the audio codec depends mainly on the selected sample rate, since the bandwidth is limited in the down and up sampling filters. These digital filters both contain several FIR and IIR low pass filters and a DC removal filter (high pass filter). A 1st order analog anti aliasing filter is implemented at the input of the microphone input to prevent aliasing in the ADC path (this feature may not be available on future revisions for the part). A 3rd order smoothing filter is implemented in the DAC path, between DAC and speaker driver stage to reduce the spurious frequencies at the speaker outputs.

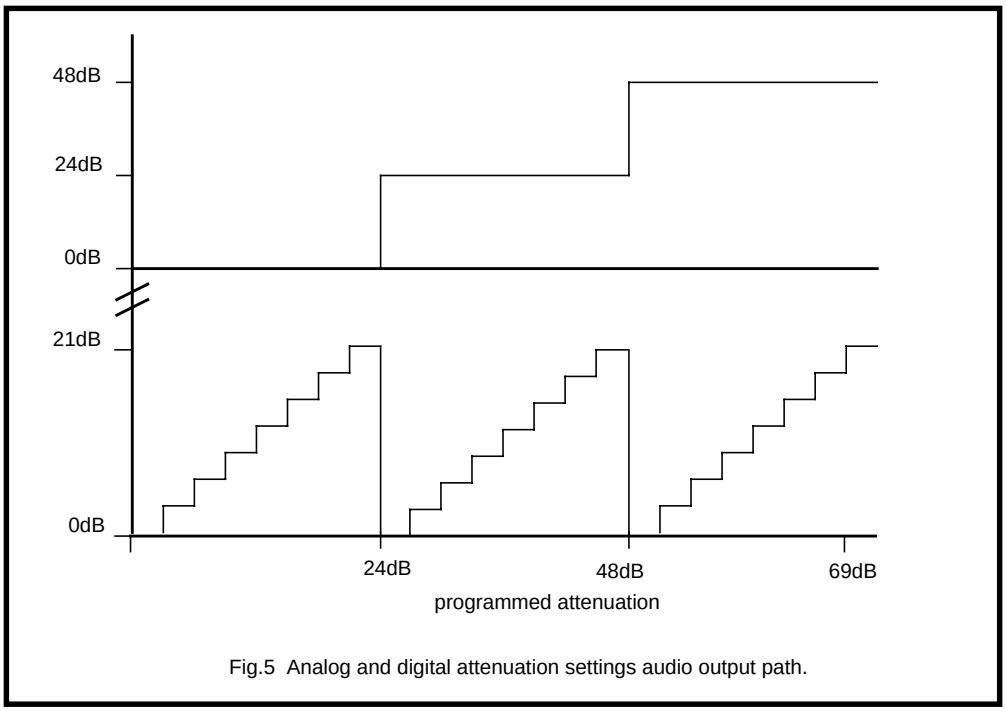


Fig.5 Analog and digital attenuation settings audio output path.

The output level can be attenuated in 3 dB steps down to -69 dB. The first 8 attenuation steps (0 to 21 dB) are implemented in the analog domain. The digital up sample filter contains a 24 dB and a 48 dB attenuation setting. This arrangement preserves the resolution, thus the 'audio quality' of the audio output signal for attenuation settings till 21 dB.

The speaker driver is muted when AUDIO_MUTE in the audio control register B is set. The speaker driver will remain activated in that case, however no signal is produced by the speaker driver circuit.

The speaker driver is designed to directly drive a bridge tied load (BTL). This yields the highest output power and this arrangement does not require external DC blocking capacitors. The speaker driver also accepts single ended connection of a speaker, in which case the maximum output power is reduced to a quarter of the BTL situation. Consequently this way of connecting the speaker to the speaker driver reduces the power consumption of the speaker driver in the UCB1100 by a factor of 2. Fig.6 shows possible ways to connect a speaker to the UCB1100. Loading the amplifiers with a capacitive load may cause high frequency oscillations and should be done cautiously.

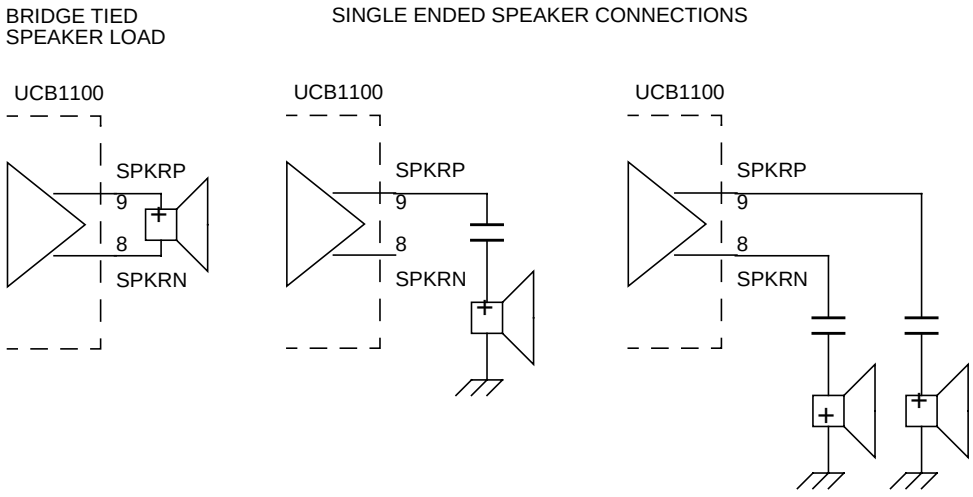


Fig.6 Possible speaker connections.

The audio input and output path are activated independently; the input path is enabled when AUDIO_IN_ENA is set, the output path is enabled when AUD_OUT_ENA is set in the audio control register B. This provides the user the means to reduce the current consumption of the UCB1100 if one part of the audio codec is not used in the application.

The audio codec has a loopback mode for system test purposes, which is activated when the AUDIO_LOOP bit in the audio control register B is set. This is an analog loopback which internally connects the output of the audio output path to the input of the audio input path, (see Fig.3). In this mode the normal microphone input is ignored, but the speaker driver can be operated normally.

TELECOM CODEC

The telecom codec contains an input channel, built up from a 64 times oversampling sigma delta analog to digital converter (ADC) with digital decimation filters, programmable attenuation and built-in sidetone suppression circuit.

The output path consist of a digital up sample filter, a 64 time oversampling 4 bit digital to analog converter (DAC) circuit followed by a differential output driver, capable of directly driving a 600 Ω isolation transformer. The output path includes a mute function. The telecom codec also incorporates a loopback mode, in which codec output path and the input path are connected in series.

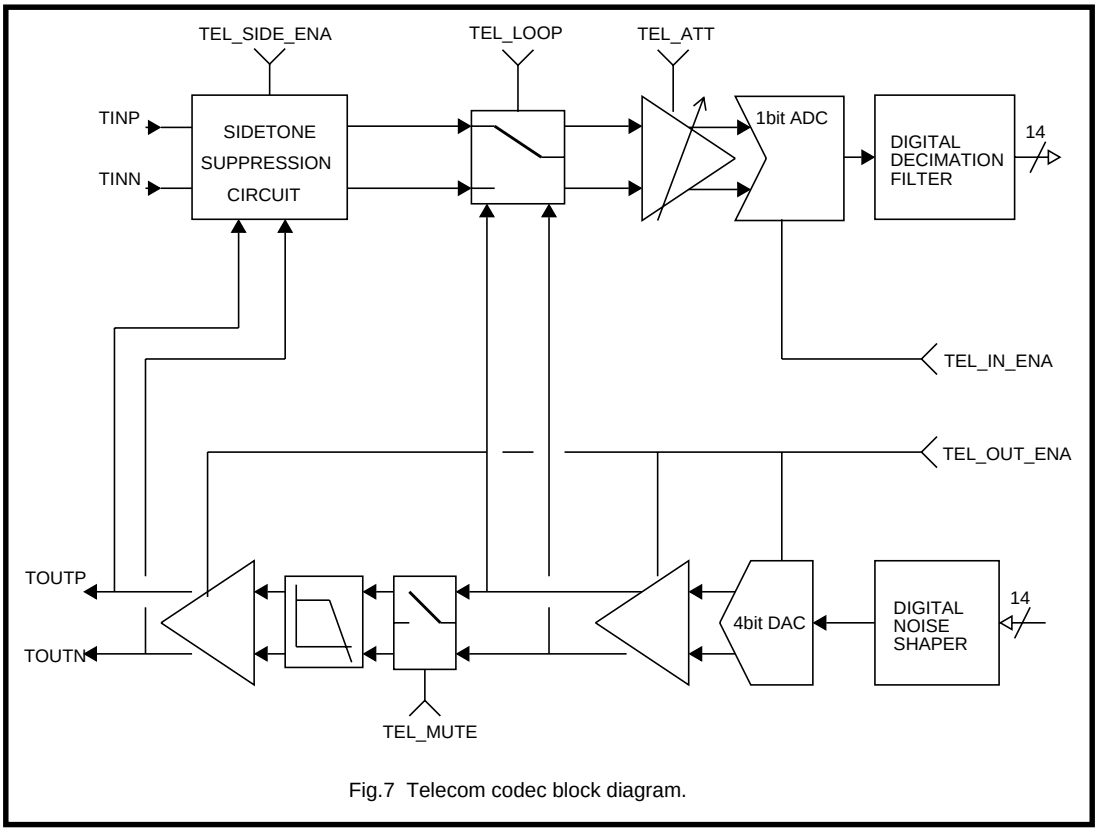


Fig.7 Telecom codec block diagram.

The telecom sample rate (f_{st}) is derived from the SIB interface clock pin (SIBCLK) and is programmable through the SIB interface. The telecom sample rate is given by the following formula:

$$f_{st} = \frac{(2 \times F_{SIBCLK})}{(64 \times TEL\_DIV[n])} \qquad (15 < TEL\_DIV[n] < 128)$$

For example, a SIBCLK of 9.216 MHz, with a divisor of 40, results in a telecom sample rate of 7.2 kHz. Both the rising and the falling edges of the SIBCLK are used in case TEL_DIV[n] is set to an odd number. In that case a 50% duty cycle of the SIBCLK signal is mandatory to obtain time equidistant sampling.

The input path of the telecom codec has a programmable attenuation. It also implements a voice band filter, which consists of an digital low pass filter, which is a part of the decimation filter. Therefore the pass band of the voice band

filter is determined by the selected telecom codec sample rate. This voice band filter is activated by setting TEL_VOICE_ENA in the telecom control register B. The resulting telecom input filter curves are given in Fig.37 and Fig.38.

The output section of the telecom codec is designed to interface with a 600 Ω line through an isolation transformer. The built in mute function is activated by TEL_MUTE in the telecom control register B. The output driver remains active in the mute mode, however no output signal is produced. Loading the drivers with a capacitive load may cause high frequency oscillations and should be done cautiously.

TOUCH SCREEN MEASUREMENT MODES

The UCB1100 contains an on chip interface for a 4 wire resistive touch screen. This interface supports three modes of touch screen measurements: position, pressure and plate resistance.

POSITION MEASUREMENT

Two position measurements are needed to determine the location of the pressed spot. First an X measurement, secondly a Y measurement. The X plate is biased during the X position measurement of the X plate and the voltage on one or both Y terminals (TSPY, TSMY) measured. The circuit can then be represented by a potentiometer, with the TSPY and/or TSMY electrode being the 'wiper'. The measured voltage on the TSPY/TSMY terminal is proportional to the X position of the pressed spot of the touch screen.

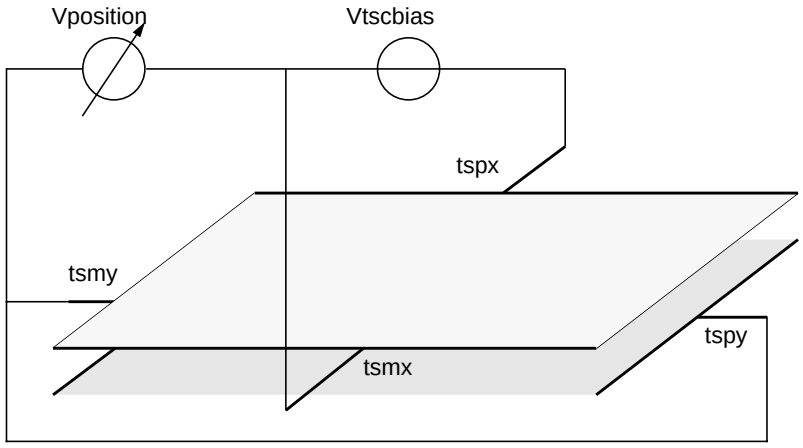


Fig.8 Touch screen setup for position measurement.

In the Y position mode the X plate and Y plate terminals are interchanged, thus the Y plate is biased while the voltage on the TSPX and/or TSMX terminal is measured.

PRESSURE MEASUREMENT

The pressure used to press the touch screen can be determined. In fact the contact resistance between the X and Y plate is measured, which is a good indication of the size of the pressed spot and the applied pressure. A soft stylus, e.g. a finger, leads to a rather large contact area between the two plates when a large pressure is applied. A hard stylus, e.g. a pen, leads to less variation in measured contact resistance since the contact area is rather small.

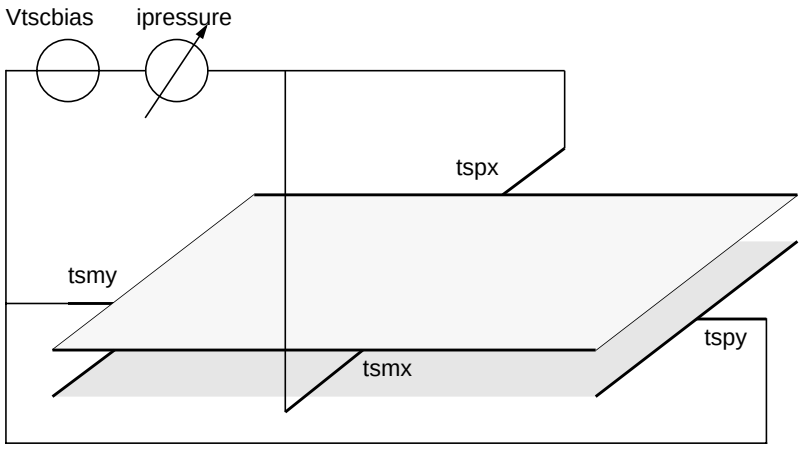


Fig.9 Touch screen setup for pressure measurement.

One plate is biased at one or both terminals during this pressure measurement, whereas the other plate is grounded, again on one or both terminals. The current flowing through the touch screen is a direct indication for the resistance between both plates. A compensation for the series resistance, formed by the touch screen plates itself will improve the accuracy of this measurement.

PLATE RESISTANCE MEASUREMENT

The plate resistance of a touch screen varies typically a lot due to processing spread. Knowing the actual plate resistance makes it possible to compensate for the plate resistance effects in pressure resistance measurements. The plate resistance decreases when two or more spots on the touch screen are pressed. In that case a part of one plate, e.g. the X plate is shorted by the other plate, which decreases the actual plate resistance

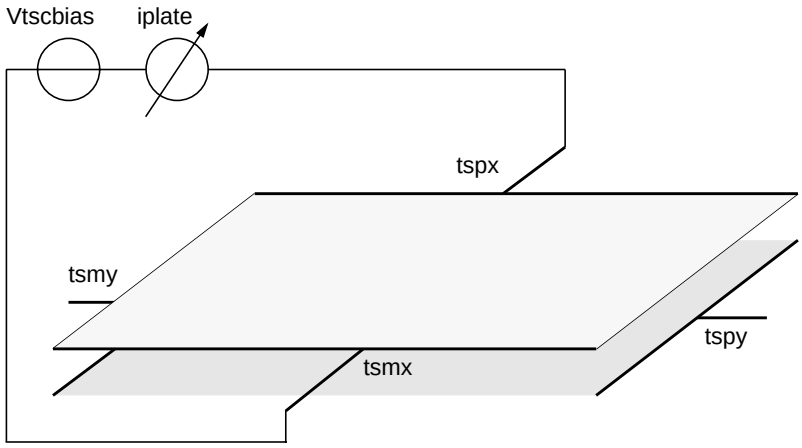


Fig.10 Touch screen setup for plate resistance.

The plate resistance measurement is executed in the same way as the pressure resistance measurement. In this case only one of the two plates is biased and the other plate is kept floating. The current through the connected plate is again a direct indication of the connected resistance.

TOUCH SCREEN INTERFACE

The UCB1100 contains a universal resistive touch screen interface for 4-wire resistive touch screen, capable of performing position, pressure and plate resistance measurements. In addition the touch screen can be programmed to generate interrupts when the touch screen is pressed. The last mode is also active when the UCB1100 is set in the stand-by mode.

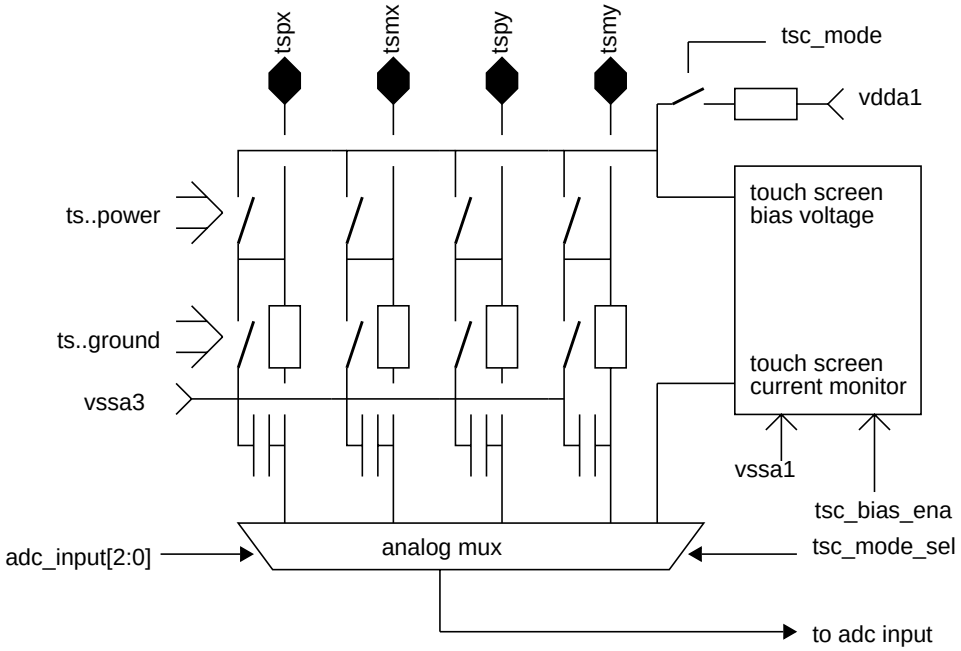


Fig.11 Block diagram of the touch screen interface.

The touch screen interface connects to the touch screen by four wires: TSPX, TSMX, TSPY and TSMY. Each of these pins can be programmed to be floating, powered or grounded in the touch screen switch matrix. The setting of each touch screen pin is programmable through the touch screen control register. Possible conflicting settings (grounding and powering of a touch screen pin at the same time) are detected by the UCB1100. In that case the UCB1100 will ground the touch screen pin.

The UCB1100's internal voltage reference (V_{ref}) is used as reference voltage for the touch screen bias circuit. This makes the touch screen biasing independent of supply voltage and temperature variations. Four low pass filters, one on each touch screen terminal, are built in to minimize the noise coupled from the LCD into the touch screen signals. An LCD typically generates large noise glitches on the touch screen, since they are closely coupled. The influence of the glitches can nevertheless be minimized by performing measurements when the LCD is quiet. This can be done by synchronizing the measurement and the video driver with the ADCSYNC pin.

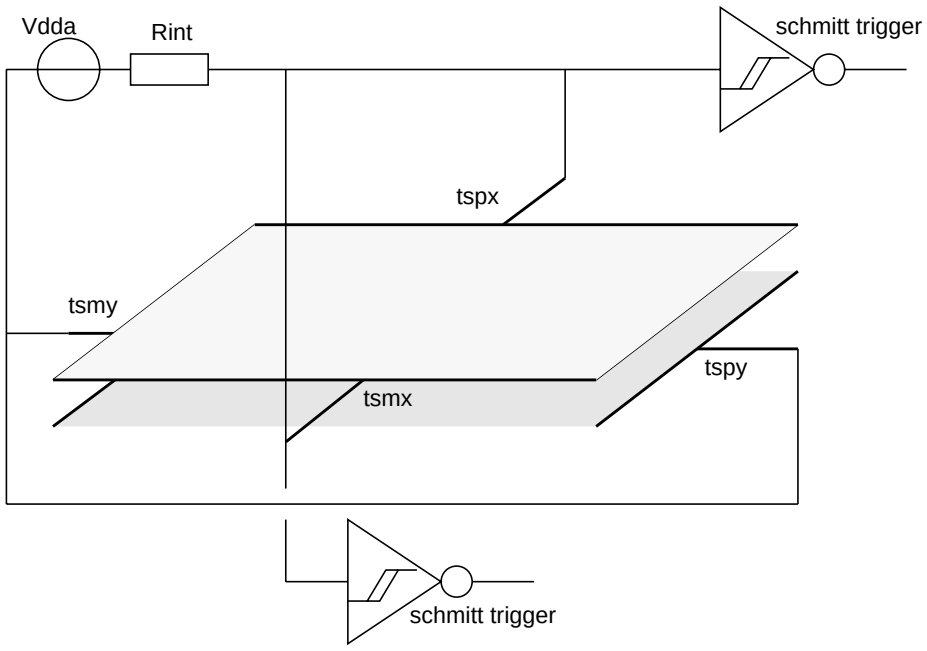


Fig.12 Touch screen setup for interrupt detection.

In addition to the measurements mentioned above, the touch screen can also act as an interrupt source. In this mode the X plate of the touch screen has to be powered and the Y plate has to be grounded. In this case the touch screen is not biased by the active touch screen bias circuit, but by a resistor to V_{DDA1}. This configuration simply biases the touch screen and the UCB1100 does not consume power unless the touch screen is touched. The voltage on the X plate terminals drops if the screen is pressed. This voltage drop is detected by Schmitt-trigger circuits, of which the outputs are connected to the interrupt control block. A touch screen interrupt is generated either when the touch screen is pressed (falling edge enabled) or when the touch screen is released (rising edge enabled). It can be used to activate the system around the UCB1100 to start a touch screen read-out sequence. The internal Schmitt-trigger circuits are connected to the TSPX and TSMX signals after the built in low pass filters. This reduces the number of spurious interrupts, due to the coupling between the LCD screen and the touch screen sensors.

Each of the four touch screen signals can be selected as input for the built in 10 bit ADC, which is used to determine the voltage on the selected touch screen pin. The flexible switch matrix and the multi- functional touch screen bias circuit enables the user of the UCB1100 to set each desired touch screen configuration.

The setting of the touch screen bias circuit and the ADC input multiplexer is determined by the setting of TSC_MOD[n] in the touch screen control register according the following table.

TOUCH SCREEN MODE SELECTION

TSC_MODE[N]	SELECTED BITS	TOUCH SCREEN BIAS SOURCE	ADC MULTIPLEXER SETTING
00	interrupt	resistor to V_{DDA1}	defined by ADC_INPUT[n]
01	pressure	touch screen bias circuit	touch screen current monitor
10	position	touch screen bias circuit	defined by ADC_INPUT[n]
11	position	touch screen bias circuit	defined by ADC_INPUT[n]

SUMMARY OF TOUCH SCREEN MODES; note 1

TOUCH SCREEN MEASUREMENT	TSPX	TSMX	TSPY	TSMY	TOUCH SCREEN MODE	TOUCH SCREEN BIAS
X position	powered(2)	grounded(2)	ADC_INPUT[n]	ADC_INPUT[n]	position	enabled
Y position	ADC_INPUT[n]	ADC_INPUT[n]	powered(2)	grounded(2)	position	enabled
pressure - 1	powered(2)	powered(2)	grounded(2)	grounded(2)	pressure	enabled
pressure - 2	powered	floating	grounded	floating	pressure	enabled
pressure - 3	floating	grounded	powered	floating	pressure	enabled
pressure - 4	floating	powered	floating	grounded	pressure	enabled
pressure - 5	grounded	floating	floating	powered	pressure	enabled
X-plate resistance	powered(2)	grounded(2)	floating	floating	pressure	enabled
Y-plate resistance	floating	floating	powered(2)	grounded(2)	pressure	enabled
interrupt	powered	powered	grounded	grounded	interrupt	disabled(3)

Note

1. Control register address 9 is used for touch screen mode selection.
2. The powered and grounded touch screen pins may be interchanged.
3. In this mode, the touch screen bias must be disabled by the user to prevent false interrupts.

10 BIT ADC

The UCB1100 includes a 10 bit successive approximation analog to digital converter (ADC) with built-in track and hold circuit and an analog multiplexer to select one of the 4 analog inputs (AD0 - AD3), the 4 touch screen inputs (TSPX, TSMX, TSPY, TSMY) or the pressure output of the touch screen bias circuit. The ADC is used to read-out the touch screen inputs and it measures the voltage on the four analog high voltage inputs AD0 - AD3. The analog multiplexer contains 4 resistive dividers to attenuate the high voltage on the AD0 - AD3 inputs to the ADC input range.

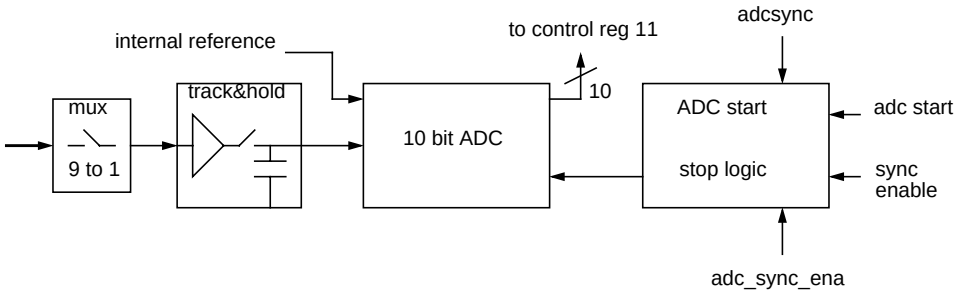


Fig.13 Block diagram of the 10-bit ADC circuit.

The ADC is controlled completely through the SIB interface, but the UCB1100 contains internal logic to ease the control of the ADC and to minimize the number of SIB frame read/write actions.

A complete ADC control sequence analog to digital conversion consists of several phases. Firstly the ADC has to be enabled, secondly the input selector must be set to the proper input, thirdly the ADC conversion has to be started and finally the ADC result has to be read from register 11.

The ADC is activated by setting ADC_ENA in register 10. The ADC circuit, including the track and hold circuit does not consume any power as long as this bit is reset. The analog input multiplexer is controlled by ADC_INPUT[n] and the ADC is actually started with the ADC_START bit. When TSPX and TSMX are in the interrupt mode, the ADC cannot be started, even to measure AD0-3.

The UCB1100 has two different modes to start the ADC conversion, which are selected by the ADC_SYNC_ENA bit. The default mode is the non-synchronization mode, in which the conversion is started directly with a 0->1 transition of ADC_START. Secondly the ADC is started at a rising edge of the signal applied to the ADCSYNC pin if ADC_SYNC_ENA is set.

The internal track and hold circuit requires a certain settling time to track the input signal correctly. This can be ensured from the software by writing first a SIB frame with the ADC multiplexer setting before the SIB frame with the ADC_START command is transferred. The UCB1100 ADC start/stop logic will detect whether the ADC input multiplexer is changed in the same SIB frame as the ADC start command is given. In that case it will delay the actual start of the ADC circuit to ensure that the track and hold settling time requirements are met. This leads to the following two timing diagrams:

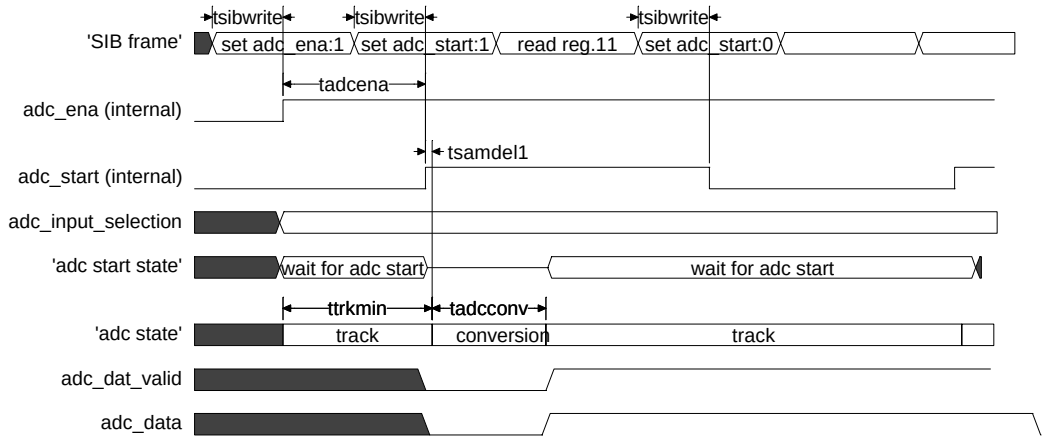


Fig.14 ADC timing sequence, non ADC sync mode, no changing ADC input multiplexer settings.

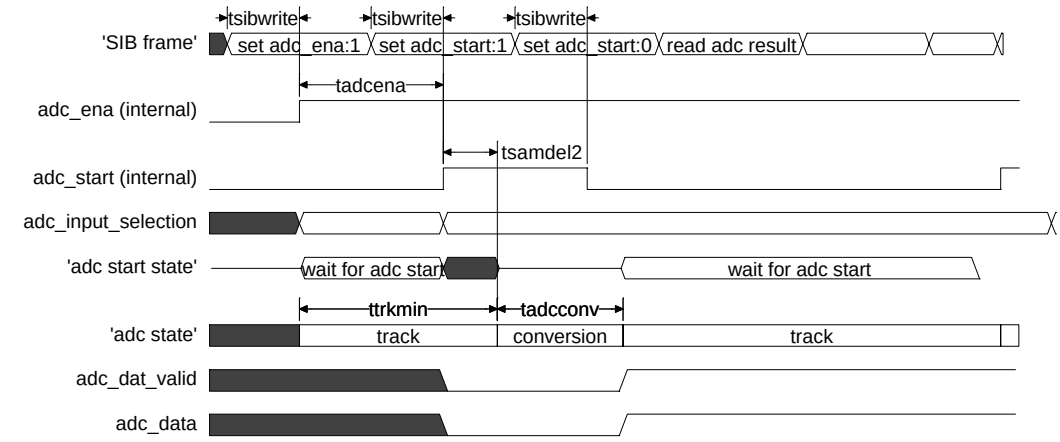


Fig.15 ADC timing sequence, non ADC sync mode, changing ADC input multiplexer settings.

The ADC timing diagrams indicate that in the non-ADC sync mode the ADC result can be read in the SIB frame following the SIB frame with the ADC start command, if the ADC multiplexer setting is not changed. If the ADC input multiplexer setting is changed, the ADC result can be read in the second SIB frame following the SIB frame with the ADC start command.

The second ADC start mode gives the opportunity to start the ADC at the rising edge of the signal connected to the ADCSYNC pin. The 0->1 transition of the ADC_START bit will arm the ADC, such that it will start in the first detected rising edge of the ADCSYNC signal. Also in this mode, the internal start/stop logic will detect whether the ADC multiplexer settings are changed simultaneously with the ADC start bit and it will add a delay to ensure sufficient setting time for the internal track and hold circuit. A rising edge of the signal connected to the ADCSYNC pin occurring during this tracking time is ignored; the ADC conversion is started on the first rising edge detected after this delay time. This leads to the following two timing diagrams of the ADC conversion.

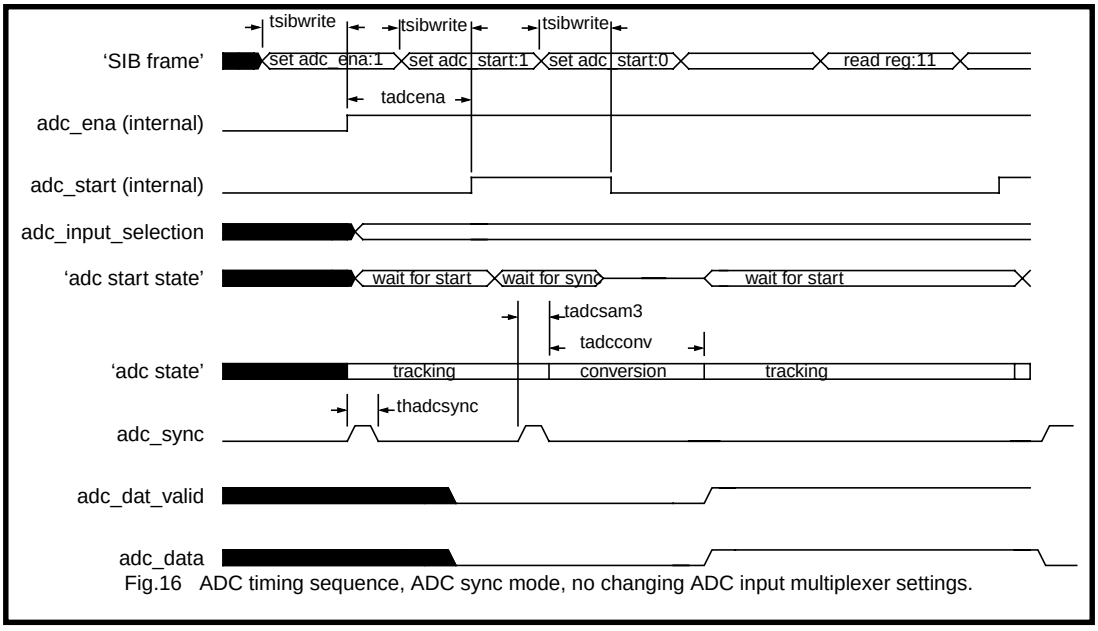


Fig.16 ADC timing sequence, ADC sync mode, no changing ADC input multiplexer settings.

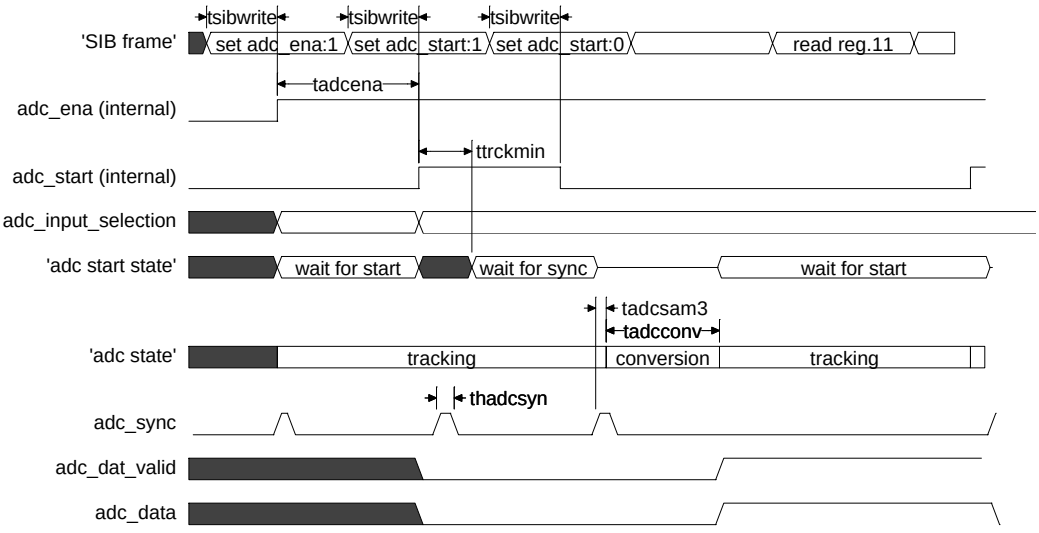


Fig.17 ADC timing sequence, ADC sync mode, changing ADC input multiplexer settings.

The ADC sync mode is particularly useful when the internal ADC has to be synchronized to the external system. Typically it is used to synchronize the read-out of the touch screen to the driving of the LCD screen, which is normally placed beneath the touch screen. Many spikes and a lot of 'noise' are superposed on the touch screen signals, due to the close coupling of the touch screen and the LCD.

The result of the conversion is stored in the register 11 of the SIB interface, after the completion of the conversion. An interrupt may be generated whenever a conversion is completed (ADC_FLA_INT and/or ADC_RIS_INT bits in register 2 and 3) to ease the synchronization between the UCB1100 and the system controller. The ADC result is reset to 0x000, whenever the ADC is started or armed till the ADC conversion is completed. ADC_DAT_VAL in the SIB register 11 indicates the status of the ADC; it equals '0' when a ADC sequence is started, which implies that the ADC result is not valid and it equals '1' when the ADC conversion is completed and the result is stored in the SIB register 11.

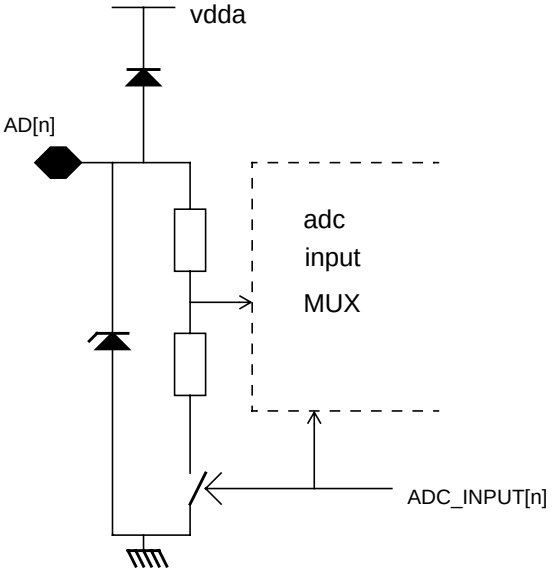


Fig.18 Block diagram of resistive dividers AD0 - AD3.

The applied voltage on the four analog inputs of the UCB1100 (AD0 - AD3) is attenuated before it is applied to the ADC input multiplexer using on chip resistive dividers.These high voltage inputs are optimized to handle voltages larger than the applied supply voltage. The built-in resistive voltage dividers are only activated if the corresponding analog input is selected. The resistive dividers are made floating when the input is not selected by the ADC input multiplexer, such that the input leakage of these high voltage analog pins is minimized. This makes these analog inputs very suitable to monitor battery voltage voltages. The diode connected to vdda will not allow to monitor voltages above vdda+0.8V. It is not present in later versions of the circuit.

ON-CHIP REFERENCE CIRCUIT

The UCB1100 contains an on chip reference voltage source, which generates the reference voltages for the 10 bit ADC and the virtual analog ground. Alternatively the UCB1100 can be driven from an external reference voltage source.

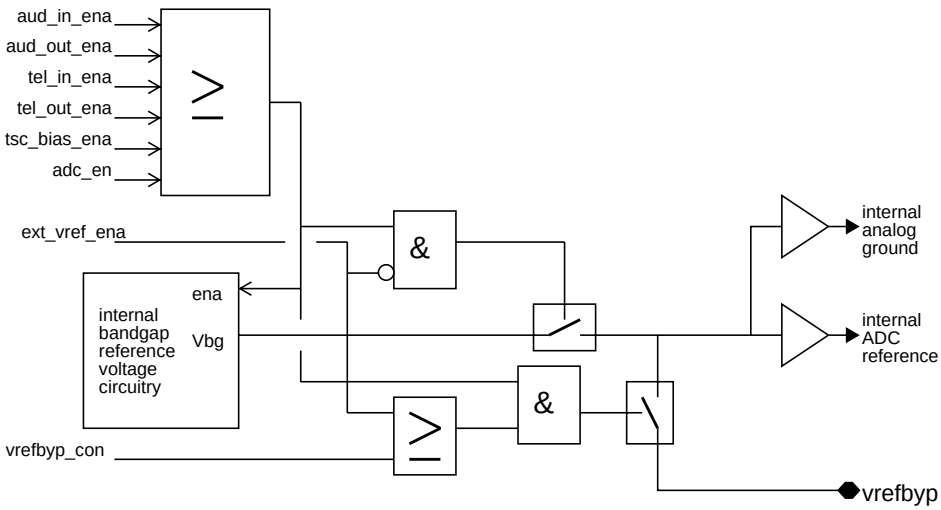


Fig.19 Block diagram of the reference circuit.

The internal reference voltage is connected to the VREFBYP pin, where an external capacitor can be connected to filter this reference voltage, if VREF_CON (register 10) is set.

An external voltage reference connected to the VREFBYP pin is used as voltage reference by the UCB1100 circuit, if the EXT_REF_ENA bit (register 10) is set. Two bits in the ADC control register determine the mode of operation of this reference voltage circuit. VREFBYP_CON connects the internal reference voltage to the VREFBYP pin, while EXT_VREF_ENA disables the internal reference voltage and switches the UCB1100 into the external voltage reference mode.

SERIAL INTERFACE BUS

The UCB1100 Serial Interface Bus (SIB) is compatible with industry standard serial ports and devices, and is designed to connect directly to a system controller. The SIB protocol allows one or more slave devices to be connected to the system controller. The data transfer is always synchronous and it is frame based. The SIB interface consists of four signals: SIBDIN, SIBDOUT, SIBCLK and SIBSYNC.

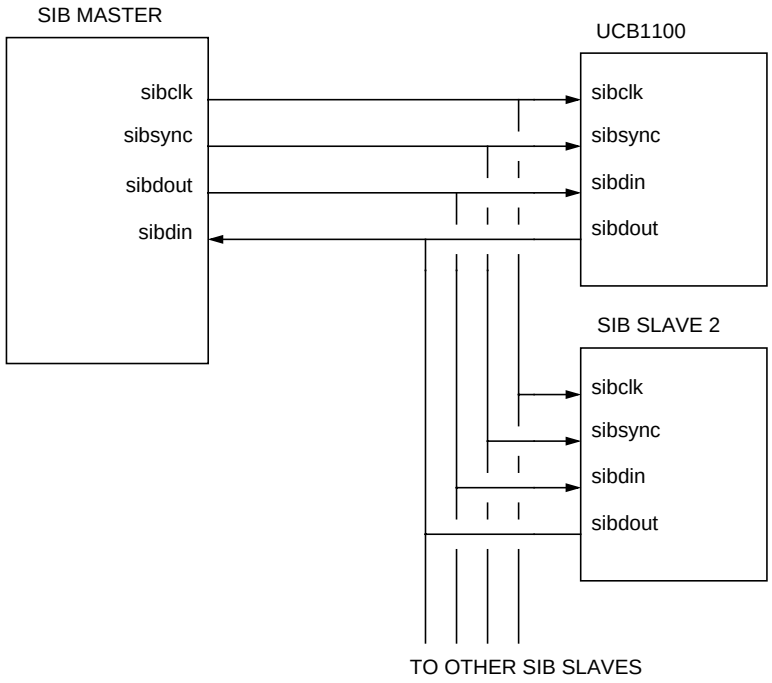


Fig.20 Typical connection between the UCB1100 and the system controller.

Each SIB frame consists of at least 64 clock cycles. Typically 128 bits are used, divided into 2 sub frames of 64 bits each. The first word (the bits 0 to 63) is read and/or written by the UCB1100, the remaining bits may be used for communication between the system controller and another slave device. The SIBDOUT pin of the UCB1100 is default -stated for the bit 64 and higher in the SIB frame to prevent bus conflicts with other slave devices. However when SIB_ZERO (control register 1) is set, the SIBDOUT pin is forced to zero from bit 64 onwards to prevent the SIBDOUT line from floating. This feature is needed when the UCB1100 is the only slave device connected to the bus.

The UCB1100 always samples incoming data on the SIBDIN pin on the falling edge of SIBCLK and it outputs data on the SIBDOUT pin on the rising edge of the SIBCLK. The start of a new SIB frame is indicated by a pulse on the SIBSYNC line just before the start of this new SIB frame.

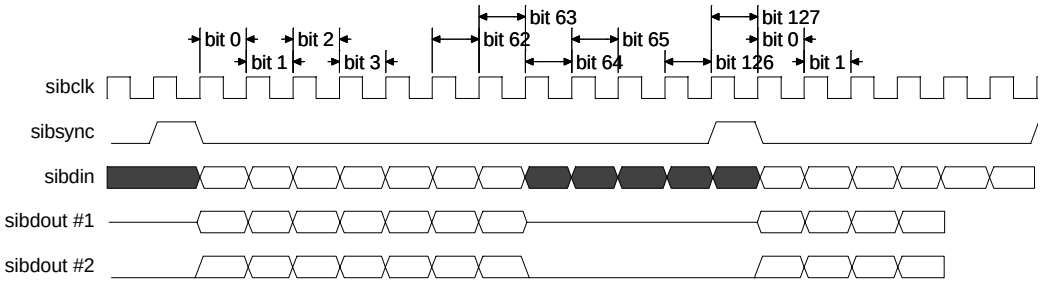


Fig.21 Serial data transmission of the UCB1100

The applied clock signal to the SIBCLK pin is used as clock signal inside the UCB1100; all internal clock signals are derived from that. It is required that the SIBCLK signal is applied if one or more analog or digital functions are activated in the UCB1100; only the interrupt controller is implemented asynchronously. SIBCLK may be stopped when all digital and analog functions are disabled; in that case the lowest possible power consumption is met. The SIBCLK should not be stopped during a SIB frame, but only at the end of the SIB-frame, to ensure that all analog and digital functions are stopped properly.

Note: The interrupt controller is still active, due to its asynchronous implementation. The UCB1100 can therefore still generate interrupts to the system controller, when the SIBCLK is stopped.

The generation of the audio and telecom sample clocks requires that the SIBCLK signal is symmetrical: a non symmetrical SIBCLK will lead to non equidistant sample moments, when an odd frequency divisor is set in either of the audio or telecom control register.

SIB DATA FORMAT

The first 64 bits in the SIB-frame are read and written by the UCB1100 and they contain both audio and telecom codec data fields, several control bits and a control register data field as is defined in table below.

SIB DATA FORMATS

SIB FRAME BIT	SIBDIN FIELD DEFINITION	SIBDOUT FIELD DEFINITION
0 - 11	audio input path data (12 bits); bit 0 = MSB	audio output path data (12 bits); bit 0 = MSB
12 - 16	not read but reserved	fixed ‘0’
17 - 20	control register address (4 bits); bit 17 = MSB	control register address (4 bits); bit 17 = MSB; is a copy of the register address as present in the SIBDIN field in the same SIB frame.
21	write bit (write 1)	fixed ‘0’
22 - 29	not read but reserved	fixed ‘0’
30	audio valid sample flag	audio valid flag
31	telecom valid sample flag	telecom valid flag
32 - 47	telecom input path data (14 bits)	telecom output path data (14 bits); bit 32 MSB
48 - 63	control register write data (16 bit); bit 48 = MSB	control register read data (16 bit); bit 48 = MSB

Since the data transfer is completely synchronous, a given control register may be written many times, before the device feeding the data has a chance to change the control bits. The UCB1100 does detect whether the data is changed or not.

CONTROL REGISTER DATA TRANSFER

The last 16 bits of the UCB1100 word is made up of control register data. The selection of the control register and whether it is read or written is defined by the control register address field [bit 17:20] and the “write” bit [bit 21]. For a read action on the a control register, the control register address field has to be set to the desired control register address and the “write” bit has to be set to zero in the SIBDIN stream, The read data is sent by the UCB1100 within the control register data field of SIBDOUT during the same frame as the read request occurred. In addition, during a read cycle, the control register data field of SIBDIN is ignored by the UCB1100 which implies that no modifications of the UCB1100 settings can be performed when the “write” bit equals zero in the SIBDIN data-stream.

For a write cycle (“write” bit = 1), the control register data contents of SIBDIN are written to the UCB1100 register selected by the register address field after receipt of the complete first word (the update is performed during the 64th bit in the SIB frame). This implies that the control register data contents of SIBDOUT data-stream in a SIB frame represents the previous contents of the selected control register.

The control register address in the SIBDOUT data-stream is a copy of the selected control register in the SIB data-stream. These bits show an additional delay since they pass additional circuit in the UCB1100.

The control register data is actually written in the control registers after the transfer of the first SIB word is completed. This implies that the control register data is updated during bit 64 of the SIB frame. The control data is only updated when the write bit is '1' in the SIB frame. The control data will not be updated when the write bit equals '0'. This simplifies the read out of control register data, since it is not required to send 'valid' data in the control register data field when a control register is read, if the write bit is kept at '0'.

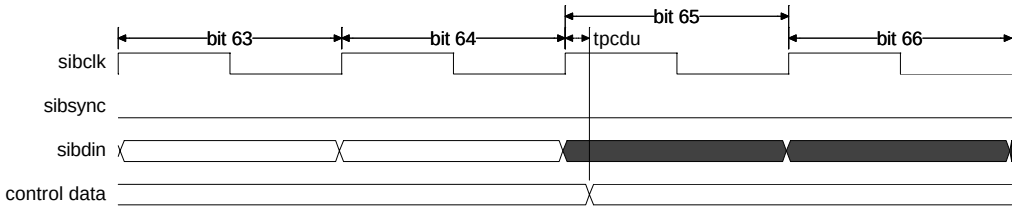


Fig.22 Control register update timing.

The control register data in the SIBDOUT stream is sampled just before the SIB frame is started. This implies that the returned control register data represents the 'old' control data, in case new data was provided in the SIBDIN data stream.

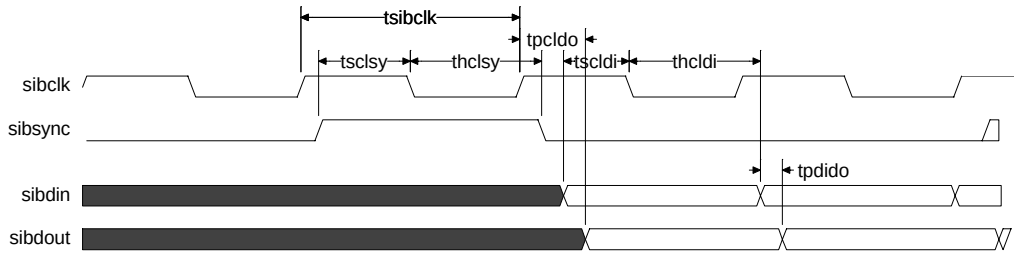


Fig.23 Timing definitions SIB interface

GENERAL PURPOSE I/O

The UCB1100 has 10 programmable digital input/output (I/O) pins. These pins can be independently programmed as input or output using IO_DIR[0:9] in control register 1. The output data is determined by the content of IO_DATA[n] in control register 0, while the actual status of these pins can be read from the IO_DATA[n] bits in control register 0.

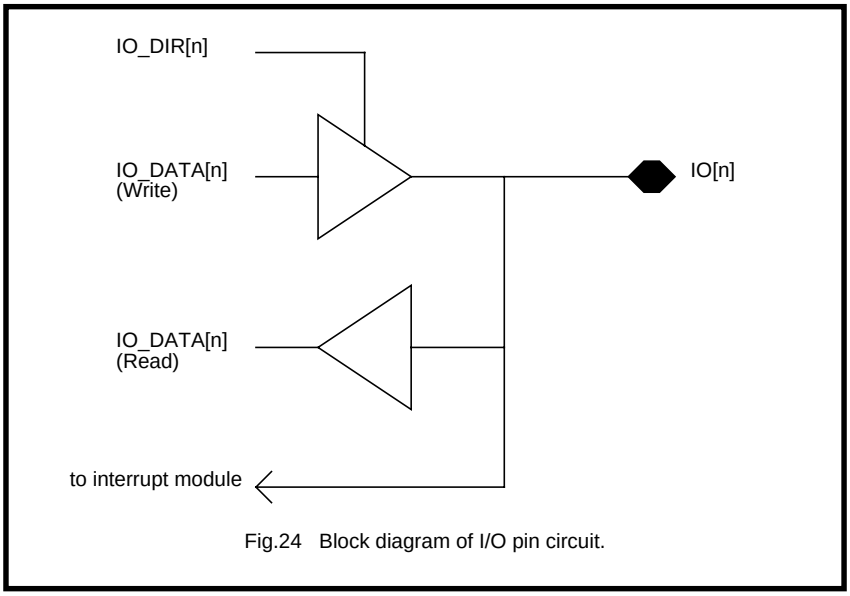


Fig.24 Block diagram of I/O pin circuit.

The data on the IO0-IO9 pins are feed into the interrupt control block, where they can generate an interrupt on the rising and/or falling edge of these signals.

INTERRUPT CIRCUIT

The UCB1100 contains a programmable interrupt control block, which can generate an interrupt for a '0' to '1' and/or a '1' to '0' transition on one or more of the IO0-IO9 pins, the audio and telecom clip detect, the adc_ready signal and the TSPX and TSMX signals. In order for the TSPX and TSMX interrupts to work properly, it is recomanded to activate the TSC_BIAS_ENA (bit 11 or reg 9) every 30s or so. This can be done while in interrupt mode.

The interrupt generation mode is set by IO_RIS_INT[n] in register 2 and INT_FAL_ENA[n] in control register 3. The actual interrupt status of each signal can be read from the control register 4. The interrupt status is cleared whenever a '0' to '1' transition is written in control register 4 for the corresponding bit. Clearing the Nth interrupt bit will also clear the bit N+1. This should be fixed in the next revision of the circuit.

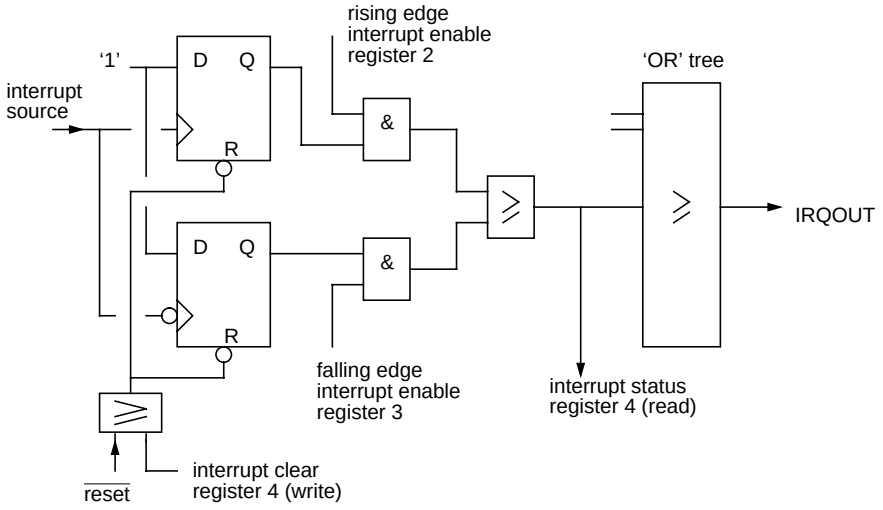


Fig.25 Block diagram of the interrupt controller.

The IRQOUT pin presents the 'OR' function of all interrupt status bits and can be used to give an interrupt to the system controller.

The interrupt controller is implemented asynchronously. This provides the possibility to generate interrupts when the SIBCLK is stopped, e.g. an interrupt can be generated in power down mode, when the touch screen is pressed or when the state of one of the IO pins changes.

RESET CIRCUIT

$\overline{\text{RESET}}$ is captured in the UCB1100 using a asynchronous pulse stretching circuit. $\overline{\text{RESET}}$ may be pulled down when the SIBCLK is still stopped. The internal circuit remembers this reset signal and generates an internal reset signal for at least 5 SIBCLK periods.

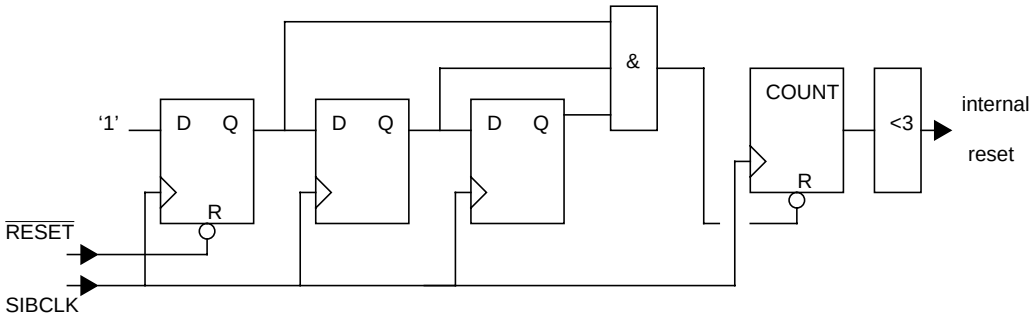


Fig.26 Block diagram of the reset circuit.

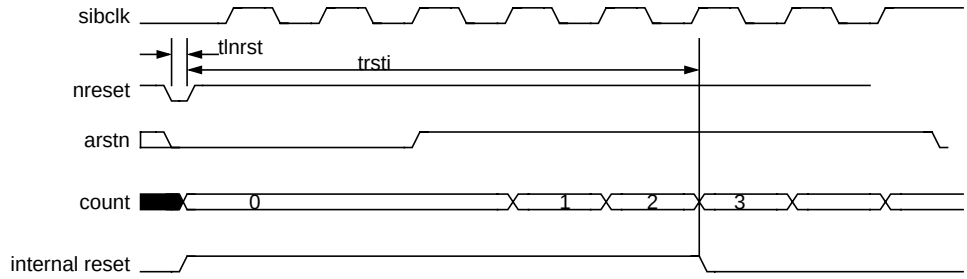


Fig.27 Timing diagram of the reset circuit.

POWER ROUTING STRATEGY

The UCB1100 has nine power supply pins, since the UCB1100 contains five power supply regions within the circuit. The analog and digital parts have their separate power supplies to reduce the interference between these parts. The speaker driver circuit is powered separately (V_{DDA2}/V_{SSA2}) from the other analog circuit parts and the touch screen switch matrix has its own ground pin (V_{SSA3}). This separation in the analog part reduces the interference between the speaker driver and the touch screen switch matrix, which has relatively large and fluctuating current consumption and the remaining parts of the analog circuit.

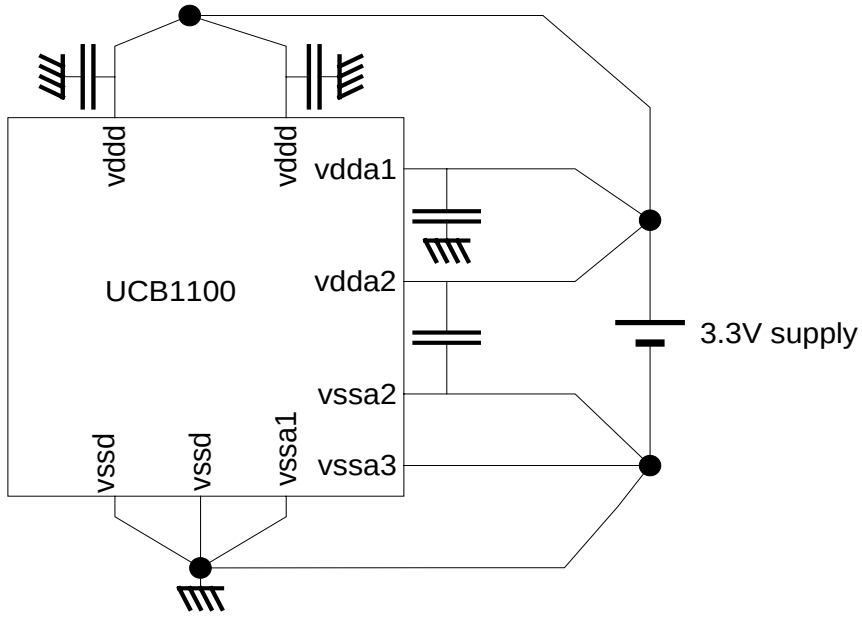


Fig.28 Recommended power supply connection strategy, single power supply systems.

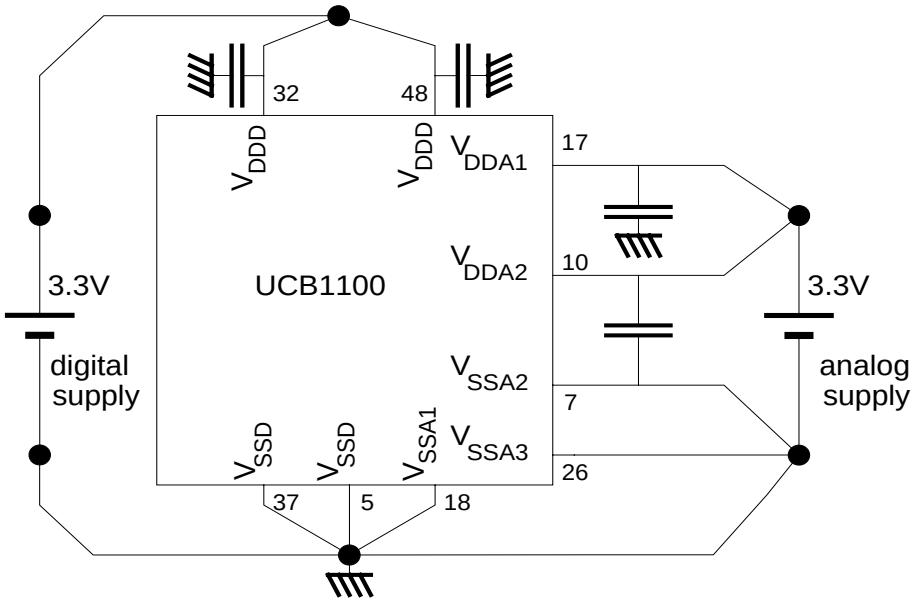


Fig.29 Recommended power supply connection strategy, dual power supply systems.

The V_{SSD} pins and the V_{SSA1} pin are connected within the UCB1100 circuit. It is recommended to connect the V_{SSD} pins and the V_{SSA1} directly to a ground plane on the PCB. The split in power supply connections should be maintained on the PCB to get optimal separation. Fig.28 shows the recommended PCB power supply strategy if only one single supply is used, while Fig.29 shows the recommended power supply connection for a dual power supply system, with separate analog and digital supplies.

APPLICATION INFORMATION

In this chapter some application information is contained. More information will be available when an Application Note on UCB1100 is published.

Sidetone suppression circuit

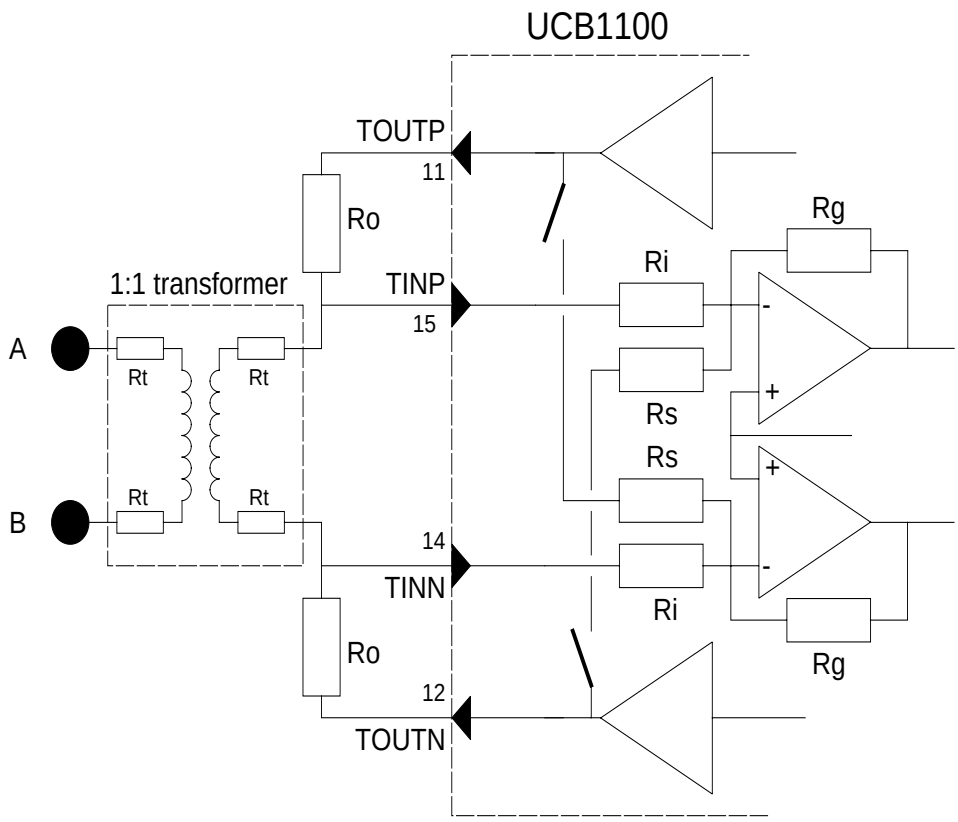


Fig.30 Typical telecom codec sidetone suppression circuit (without protection circuits).

An important built-in feature of the telecom codec is the sidetone suppression circuit. The sidetone suppression circuit is activated when TEL_SIDE_ENA in the telecom control register B is set. The telecom input signal contains a large part of the telecom output signal, when the sidetone suppression circuit is disabled. The available dynamic range of the telecom input is occupied largely by the telecom output voltage.

The sidetone suppression circuit subtracts a part of the telecom output signal from the telecom input signal when activated. The available dynamic range is in that case used more effectively than without sidetone suppression.

The built in side tone suppression circuit, shown in Fig.30, has a fixed subtraction ratio, set be the resistors R_s and R_i, which equals 600/456. This ratio is calculated from the following relations.

The impedance seen by the telephone line equals:

$$Z_{line} = 2 \times \left(R_t + R_t + \frac{R_o \times R_i}{R_0 + R_i} \right),$$

in which R_t represents winding resistance of the transformer, divided by 2. Assuming $R_i >> R_o$ then

$$R_{line} = R_t + R_t + R_o = 600/2 = 300\Omega$$

A typical transformer has 156 Ω winding impedance, thus R_o should be 144 Ω. The ratio of the telecom input and output voltage is therefore:

$$V_{i(tel)} = V_{o(tel)} \times \frac{156 + 300}{156 + 300 + 144} = V_{o(tel)} \times \frac{456}{600}$$

Codec data transfer

The UCB1100 codec operates at samples which depend on the applied SIBCLK frequency and the programmed audio and telecom divisors. The codec data transfer between the UCB1100 and the system controller has to be synchronized with the UCB1100 sample counters and the SIB bus data transfer protocol to prevent conversion errors, resulting in high distortion.

Correct codec data transfer is obtained easily when the UCB1100 is connected to one of the controllers in the PR3000 series, but the UCB1100 can also be connected to other controllers, if the following data protocol is used.

START OF CODEC DATA TRANSFER

The UCB1100 internal sample counters are started at the beginning of the first SIB frame following the SIB frame in which the codec input and/or output path is enabled. This implies that the sample rate divisor has to be programmed before the codec input and/or output path is enabled, Fig.31. Changing the sample rate on the fly, that is without disabling both the codec input and output path before the divisor is reprogrammed, will disturb the codec data transfer synchronisation between the UCB1100 and its controller and is therefore not allowed.

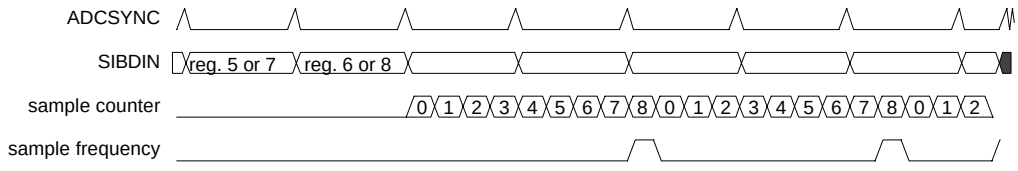


Fig.31 Start-up sequence of the codec, TEL_DIV[n] = 9.

CODEC DATA TRANSFER INTO THE UCB1100

Both the audio and the telecom data is transferred within the SIB frame (bit 11-0 and bit 47-32). This data is accompanied by two data valid flags (bit 30: audio data valid, bit 31: telecom data valid). The codec data in the SIB frames is only processed in the UCB1100 if the appropriate data valid flag is set in the frame; the data is discarded when the data flag equals ‘0’. Figure 32 shows the basic codec data synchronisation principle used in the UCB1100.

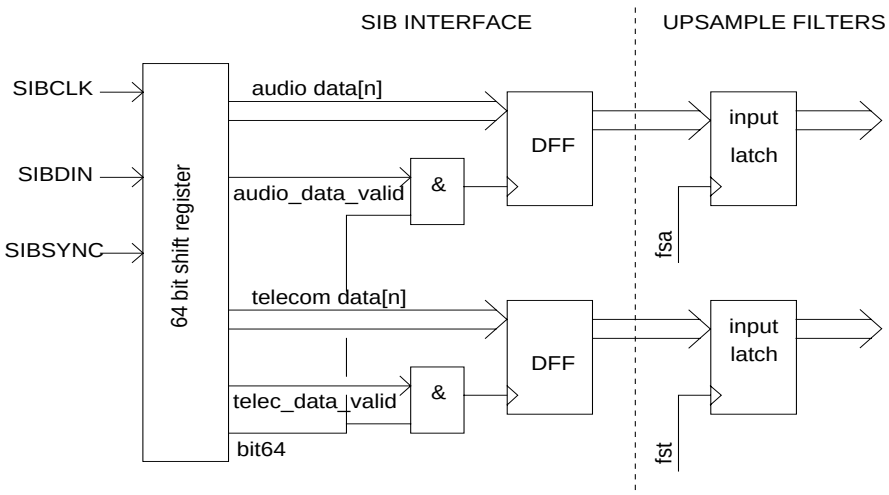


Fig.32 Codec input path data synchronisation principle.

Figure 32 shows that audio and telecom data is made available for the codec up sample filters during the 64th bit in the SIB frame. This implies that the codec data has to be transferred in one of the SIB frames preceding the codec sample moment.

Note: If the programmed divisor equals a multiple of 4, the codec data transfer is synchronized to the SIB frame repetition rate (e.g. AUD_DIV[n] = 8 ⇒1 sample is needed in 2 SIB frames, AUD_DIV[n] = 12 ⇒ 1 sample is needed in 3 SIB frames, etc.).

CODEC DATA TRANSFER FROM THE UCB1100

The data resulting from the UCB1100 codec ADC (input) paths is transfer to the system controller at the programmed codec sample rate. However the codec data is synchronized with the SIB frame repetition rate. Figure 33 shows the basic synchronisation principle used inside the UCB1100. Codec data will be present in each SIB frame produced by the UCB1100; the sample will be repeated in the following SIB frames till a new sample has become available.

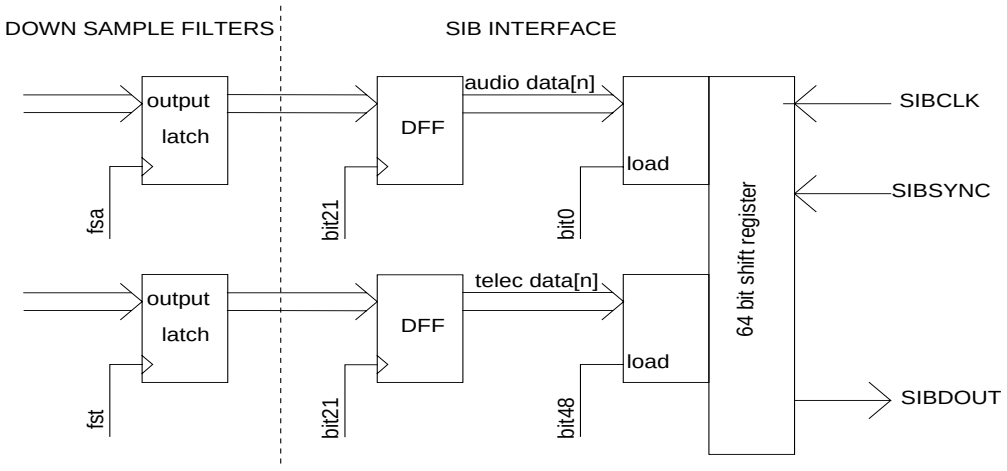


Fig.33 Synchronisation of codec samples in SIBDOUT data stream.

The codec samples in the SIBDOUT stream are also accompanied by a audio and telecom data valid bit (bit 30 and bit 31). These data valid flags are zero if the corresponding codec adc paths are disabled and during the start up period of the codec's, when unreliable samples are generated. By default (after reset), the data valid bits will be continuously '1' when reliable samples are generated.

However when DYN_VFLAG_ENA is set, the data valid bits will be '1' during one of the SIB frames, containing identical samples (this is the case when a high divisor is programmed). The audio_vflag bit will be high during the last sample in a series of identical samples, while the telecom_vflag bit is high at the first sample in a series of identical bits. An example of the timing diagram is shown in figure 34.

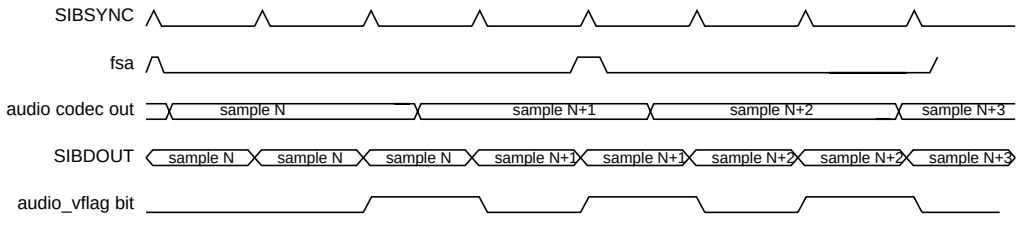


Fig.34 Audio codec data transfer, AUD_DIV[n] = 9, DYN_VFLAG_ENA = 1.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); notes 1. to 3

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+5.0	V
V_I	DC input voltage (except inputs AD0 - AD3)	–0.5	V_{DD} + 0.5	V
V_I	DC input voltage AD0 - AD3	–0.5	+8.5	V
V_O	DC output voltage	–	V_{DD} + 0.5	V
$I_{I(d)}$	diode input current	–	10	mA
$I_{O(d)}$	diode output current	–	10	mA
I_O	continuous output current, digital outputs	–	4	mA
T_{stg}	storage temperature	–55	+150	°C

Notes

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Absolute Maximum Rating section of this specification is not implied.
2. This product is manufactured in a high performance CMOS process and is ESD sensitive.
3. Parameters are valid over the ambient operating temperature unless otherwise specified. All voltages are with respect to V_{SSD} (pin 37), unless otherwise noted.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient in free air	67	K/W

DC CHARACTERISTICS

$V_{SSD} = V_{SSA1} = V_{SSA2} = V_{SSA3} = 0$ V; T_{amb} =25 °C; $f_{i(sibclk)}$ = 9.216 MHz; $V_{I(ref)}$ = 1.2 V; all voltages referenced to V_{SSD} (pin 5); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDA1}	analog supply voltage - excl. speaker driver		3.0	3.3	3.6	V
V_{DDA2}	analog supply voltage - speaker driver only		3.0	3.3	3.6	V
V_{SSA2}	analog ground - speaker driver		–0.4	0	+0.4	V
V_{SSA3}	analog ground - touch screen switch matrix		–0.4	0	+0.4	V
I_{DDD}	digital supply current(1)	full functionality	–	19	–	mA
		only audio codec activated	–	17	–	mA
		only telecom codec activated	–	19	–	mA
		only touch screen activated	–	15	–	mA
		only ADC activated	–	15	–	mA
		no functions activated; f_{sibclk} off	–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DDA1}	analog supply current(1)(2)	full functionality	–	3.8	–	mA
		only audio codec activated	–	3.0	–	mA
		only telecom codec activated	–	3.0	–	mA
		only touch screen activated	–	0.7	–	mA
		only touch screen in interrupt mode	–	–	100	µA
		only ADC activated	–	1	–	mA
		no analog functions activated	–	<10	–	µA
I_{DDA2}	total speaker driver supply(1)(2) current	speaker driver enabled	–	0.6	–	mA
		speaker driver disabled	–	–	10	µA
V_{IL}	LOW level input voltage		–0.5	–	$+0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	$0.5V_{DDD}$	V
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	–	–	$0.2V_{DDD}$	V
V_{OH}	HIGH level output voltage	I_{OH} = 2 mA	$0.8V_{DDD}$	–	–	V
$f_{i(sibclk)}$	serial interface clock frequency		0	10	15	MHz
T_{amb}	operating ambient temperature		0	–	70	°C

Notes

1. Indicative value measured during the initial characterization.
2. Excluding connected touch screen and speaker load currents.

AC CHARACTERISTICS

$V_{SSD} = V_{SSA1} = V_{SSA2} = V_{SSA3} = 0$ V; $V_{DDD} = V_{DDA1} = V_{DDA2} = 3.3$ V±10%; T_{amb} =25 °C; $V_{I(ref)}$ = 1.2 V; $f_{i(sibclk)}$ = 9.216 MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio Input; notes 1 and 2						
f_{sa}	audio sample frequency		–	–	26	kHz
$V_{I(RMS)}$	input voltage (RMS value)	0 dB gain setting	90	100	125	mV
$V_{I(BIAS)}$	DC bias voltage	MICP input	1.35	1.4	1.5	V
Z_i	input impedance		20	25	-	kΩ
$Z_{(18-20)}$	impedance MICGND - VSSA1		–	–	200	Ω
G_{step}	gain step size		1	1.5	2	dB
N_{step}	number of gain steps		–	16	–	–
G_v	gain	AC coupling enabled (AUD_OFF_CAN = 1)	15	22.5	28	dB
E_G	gain error	each gain step	–1	–	1	dB
RES	resolution		–	12	–	bit
$LE_{(d)(ADC)}$	ADC differential linearity error		–	–	1	LSB
THD	total harmonic distortion	input gain = 0 dB (AUD_GAIN = 00000);	–	–	-38	dB
		input signal = 1 mV (RMS); input gain = 22.5 dB (AUD_GAIN[n] = 01111); AC coupling enabled (AUD_OFF_CAN = 1);	–	–	-26	dB
S/N	signal-to-noise ratio	input gain = 0 dB (AUD_GAIN = 00000)	50	–	–	dB
		input signal = 1 mV (RMS); input gain = 22.5 dB (AUD_GAIN[n] = 01111);	25	–	–	dB
PBRR	pass-band ripple rejection	$f_{pla} < f_{sig} < f_{pha}$ (3)	–	–	1.2	dB
SBR	stop-band rejection	$f_{sha} < f_{sig} < 20$ kHz (3)	70	–	–	dB
D_{offset}	digital offset	no signal applied to MICP	–	–	50	LSB
Audio Output; notes 4 and 5						
$V_{O(RMS)}$	output voltage (RMS value)	attenuation = 0 dB, differentially measured between SKPRN and SPRKP	1.0	1.25	1.5	V
E_{offset}	offset error (peak-to-peak value)		–	–	100	mV
$V_{O(BIAS)}$	DC bias voltage	SPKRP/SKPRN	1.2	1.4	1.6	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{step}	attenuation step size (analog section)		2.5	3.0	3.5	dB
N_{step}	number of attenuation steps		–	24	–	–
α	attenuation		63	69	75	dB
RES	resolution		–	12	–	bit
$LE_{(d)(DAC)}$	DAC differential linearity error		–	–	1	LSB
THD	total harmonic distortion		–	–	-35	dB
		1 kΩ headphone load	–	–	-45	dB
S/N	signal-to-noise ratio	16 Ω speaker; 100 Hz to 20 kHz bandwidth	40	–	–	dB
PBRR	pass-band ripple rejection	$f_{pla} < f_{sig} < f_{pha}$(6)	–	–	1.2	dB
SBR	stop-band rejection	$f_{sha} < f_{sig} < 20$ kHz(6)	70	–	–	dB
$OBR_{(RMS)}$	out-of-band rejection (RMS value)	f > 20 kHz	–	–	50	mV
$Z_{speaker}$	speaker impedance		16	–	–	Ω
Telecom Input; notes 2 and 7						
f_{st}	sample frequency		–	–	10	kHz
$V_{I(RMS)}$	input voltage (RMS value)	differentially applied to TINN and TINP; no I/P attenuation enabled (TEL_ATT = 0)	330	370	410	mV
$V_{I(BIAS)}$	DC bias voltage	TINN/TINP	1.2	–	1.6	V
α_i	input attenuation	input attenuation enabled (TEL_ATT = 1)	5.5	6	6.5	dB
Z_i	input impedance		25	–	–	kΩ
S/N	signal-to-noise ratio		50	–	–	dB
THD	total harmonic distortion		–	–	–50	dB
$LE_{(d)(ADC)}$	ADC differential linearity error		–	–	2	LSB
RES	resolution		–	14	–	bit
PBRR	pass-band ripple rejection	$f_{plt} < f_{sig} < f_{pht}$; no voice filter(8)(16)	–	–	1.2	dB
		$f_{vht} < f_{sig} < f_{pht}$; voice filter activated(8)(16)	–	–	1.2	dB
SBR	stop-band rejection	$f_{sig} < f_{vlt}$; voice filter activated(8)(16)	30	–	–	dB
		$f_{sht} < f_{sig}$(8)(16)	50	–	–	dB
D_{offset}	digital offset	no signal applied to MICP	–	–	50	LSB
S_{sup}	sidetone suppression effectiveness	600 Ω line impedance; 1:1 transformer with 156 Ω winding resistance	20	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Telecom output; note 5						
f_{st}	sample frequency		–	–	10	kHz
$V_{O(RMS)}$	output voltage (RMS value)	differentially measured between TOUTP and TOUTN	1.35	-	1.85	V
$V_{O(BIAS)}$	DC bias voltage	TOUTP/TOUTN; telecom O/P path enabled	1.2	–	1.6	V
RES	resolution		–	14	–	bit
S/N	signal-to-noise ratio		53	–	–	dB
THD	total harmonic distortion		–	–	–50	dB
PBRR	pass-band ripple rejection		–	–	1.2	dB
SBR	stop-band rejection	$f_{sht} < f_{sig}$ (9)	70	–	–	dB
$OBR_{(RMS)}$	out-of-band rejection (RMS value)	$f > f_{st}$ (9)(16)	–	–	25	mV
$Z_{o(load)}$	load impedance		600			Ω
E_{offset}	offset error	note 10	–	–	100	mV
Touch screen						
$V_{I(BIAS)}$	bias voltage	touch screen position mode selected	1.6	1.8	2.0	V
I	touch screen current	touch screen position mode selected	10	–	–	mA
R_i	Max. touch screen resistance to generate an interrupt	touch screen interrupt mode selected	–	–	2500	Ω
R_{gs}	ground switch on resistance		–	–	50	Ω
R_{ps}	power switch on resistance		–	–	50	Ω
t_{STRTU}	start up time of touch screen bias voltage generator		–	–	25	µs
ADC; notes 11 and 12						
RES	resolution		–	10	–	bit
$V_{I(AD0-AD3)}$	full scale AD0 - AD3 inputs		7.0	7.5	8.0	V
Z_i	input impedance		50	75	100	kΩ
I_{LI}	input leakage current	$V_{ADO} = V_{AD1} = V_{AD2} = V_{AD3} = 7.5$ V			10	µA
$LE_{(d)(ADC)}$	ADC differential linearity error		–	–	1	LSB
$LE_{(i)(ADC)}$	ADC integral linearity error	5 - 95 % of full scale	–	–	2	LSB
$t_{en(ADC)}$	ADC enable time		5	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d(s)}$	sampling delay	non synchronization mode; no changing ADC multiplexer settings	–	$4t_{SIBCLK}$	–	ns
		non synchronization mode; changing ADC multiplexer settings	–	$51t_{SIBCLK}$	–	ns
		synchronization mode; rising edge ADCSYNC to sample moment	t_{SIBCLK}		$1.5t_{SIBCLK}$	ns
t_{conv}	conversion time		–	$102t_{SIBCLK}$		ns
t_{track}	tracking time		$5t_{SIBCLK}$	$49t_{SIBCLK}$	–	ns
$t_{adcsync}$	high time ADCSYNC signal		$10t_{SIBCLK}$	–	–	ns
$t_{sibwrite}$	control register update after SIBSYNC falling edge		–	$65t_{SIBCLK}$	–	ns
On-chip reference circuit						
$V_{i(ref)}$	reference voltage applied to VREFBYP		1.0	1.2	1.4	V
t_{STRTU}	start-up time of internal reference voltage circuit		–	–	$50t_{SIBCLK}$	ns
Control register data transfer						
$f_{i(sibclk)}$	SIBCLK input frequency		0	–	15	MHz
$\delta_{(sibclk)}$	SIBCLK duty factor	note 13	–	50	–	%
$t_{su(SIBSYNC-SIBCLK)}$	set-up time SIBSYNC to SIBCLK falling edge		–	15	–	ns
$t_{h(SIBSYNC-SIBCLK)}$	SIBSYNC hold time after falling edge of SIBCLK		–	10	–	ns
$t_{su(SIBDIN-SIBCLK)}$	set-up time SIBDIN to SIBCLK falling edge		–	15	–	ns
$t_{h(SIBDIN-SIBCLK)}$	SIBDIN hold time after falling edge of SIBCLK		–	10	–	ns
$t_{(SIBCLK-SIBDOUT)}$	rising edge of SIBCLK to valid SIBDOUT	note 14	–	10	–	ns
$t_{(SIBDIN-SIBDOUT)}$	valid SIBDIN to valid SIBDOUT	note 15	–	15	–	ns
Reset circuit						
$t_{W(NRESET)}$	$\overline{\text{RESET}}$ pulse width		5	–	–	ns
$t_{W(rst)}$	internal reset pulse width			$5t_{SIBCLK}$	–	ns

Notes

1. Additional test conditions: AUD_DIV[n] = 00001100; input signal 1 kHz, 90 mV (RMS); AUD_IN_ENA = 1.
2. Coding system for ADC output data is 2’s complement.
3. See Fig. 35.

4. Additional test conditions: AUD_DIV[n] = 00001100; 0 dB output attenuation; 90 % of digital full scale input voltage; 16 Ω speaker connected.
5. Additional test conditions: TEL_DIV[n] = 0101000; 0 dB output attenuation; 90 % of digital full scale input voltage; 1200 Ω load.
   Coding system for DAC input data is 2's complement.
6. See Fig. 36.
7. Additional test conditions: TEL_DIV[n] = 0101000; input signal 1 kHz, 300 mV (RMS); TEL_IN_ENA = 1; TEL_VOICE_ENA = 0.
8. See Fig. 37.
9. See Fig. 38.
10. Deviation of the analog output from 0, with 0 code input to telecom output path.
11. The ADC cannot be started or armed if the touch screen circuit is set to interrupt mode (TSC_MODE[n] = 0,0).
12. Coding system for ADC is binary offset.
13. This is a requirement when an odd divisor is set in either the audio or the telecom codec.
14. This is valid for all SIB frame bits 0 to 63, except bits 17 to 20.
15. This is valid for a the SIB frame bits 17 to 20.
16. All curves repeat around the sample frequency f_{sa} or f_{st} for audio- respectively telecom codec.

FREQUENCY RESPONSE CURVES

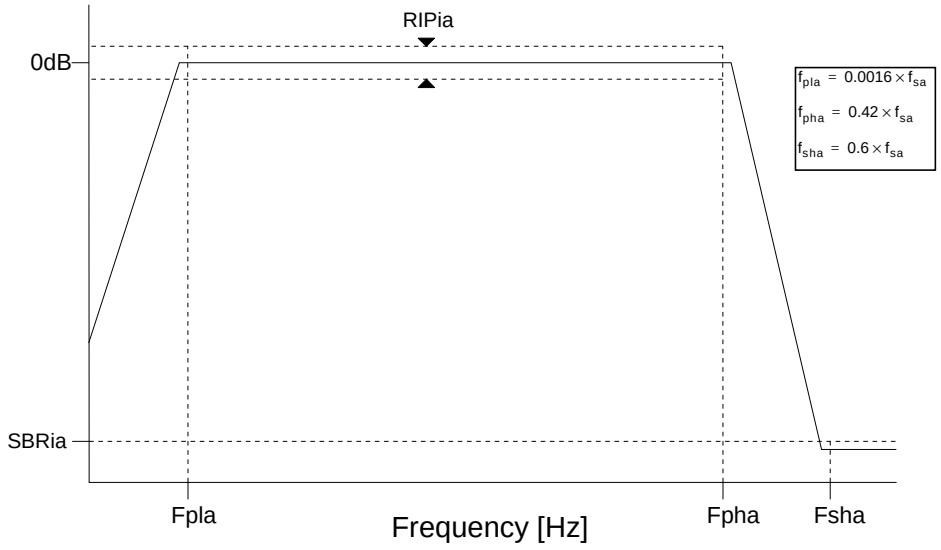


Fig.35 Audio input path frequency response.

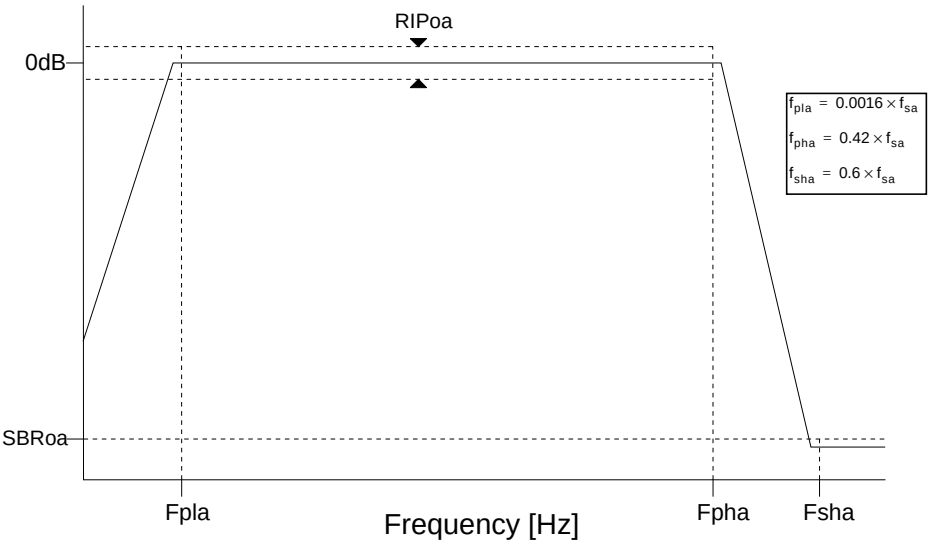


Fig.36 Audio output filter frequency response.

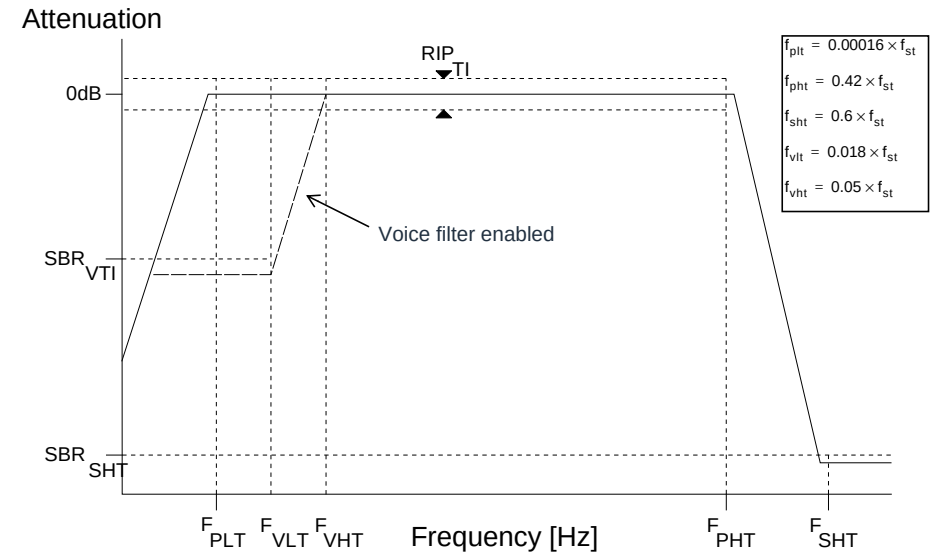


Fig.37 Telecom input frequency response

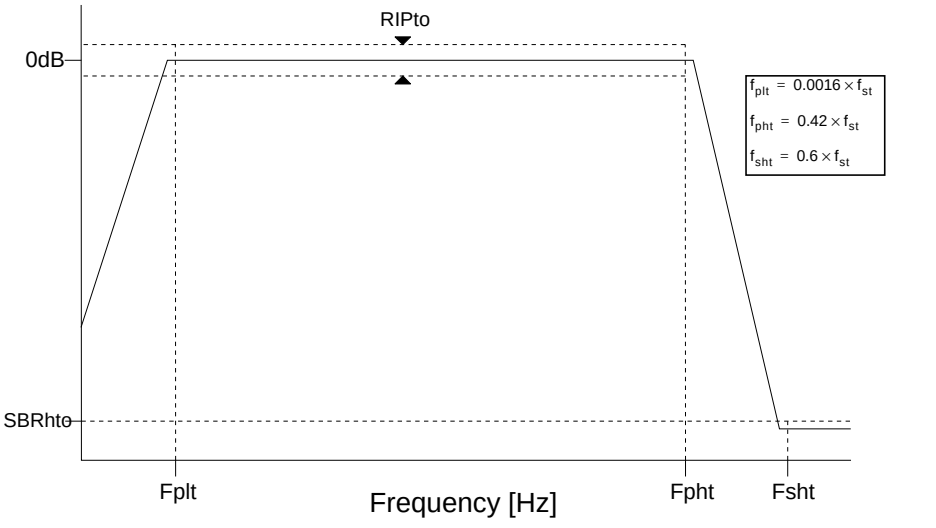


Fig.38 Telecom output frequency response.

CONTROL REGISTER OVERVIEW

BIT	MODE	SYMBOL	REMARK	RESET
Address 0: I/O port data register				
0 to 9	R/W	IO_DATA[n]	The bits in the write register provide the data of the I/O pin when programmed as output. The bits in the read register return the actual state of the associated I/O pin.	0
Address 1: I/O port direction register				
0 to 9	R/W	IO_DIR[n]	If '1', the associated I/O pin is defined as output. If '0', the associated I/O pin is defined as input.	0
15	R/W	SIB_ZERO	If '1', the SIBDOUT pin is forced '0' during the second SIB word. If '0', the SIBDOUT pin is three-stated during the second SIB word.	0
Address 2: Rising edge interrupt enable register				
0 to 9	R/W	IO_RIS_INT[n]	If '1', the rising edge interrupt of the associated I/O pin is enabled.	0
11	R/W	ADC_RIS_INT	If '1', the rising edge interrupt of the adc_ready signal is enabled.	0
12	R/W	TSPX_RIS_INT	If '1', the rising edge interrupt of the TSPX signal is enabled.	0
13	R/W	TSMX_RIS_INT	If '1', the rising edge interrupt of the TSMX signal is enabled.	0
14	R/W	TCLIP_RIS_INT	If '1', the rising edge interrupt of the telecom clip is enabled.	0
15	R/W	ACLIP_RIS_INT	If '1', the rising edge interrupt of the audio clip is enabled.	0
Address 3: Falling edge interrupt enable register				
0 to 9	R/W	IO_FAL_INT[n]	If '1', the falling edge interrupt of the associated I/O pin is enabled.	0
11	R/W	ADC_FAL_INT	If '1', the falling edge interrupt of the adc_ready signal is enabled.	0
12	R/W	TSPX_FAL_INT	If '1', the falling edge interrupt of the TSPX signal is enabled.	0
13	R/W	TSMX_FAL_INT	If '1', the falling edge interrupt of the TSMX signal is enabled.	0
14	R/W	TCLIP_FAL_INT	If '1', the falling edge interrupt of the telecom clip is enabled.	0
15	R/W	ACLIP_FAL_INT	If '1', the falling edge interrupt of the audio clip is enabled.	0
Address 4: Interrupt clear/status register				
0 to 9	W	IO_INT_CLR[n]	A '0' to '1' transition clears the interrupt of the associated I/O pin.	0
	R	IO_INT_STAT[n]	Returns the actual interrupt status of the associated I/O pin	0
11	W	ADC_INT_CLR	A '0' to '1' transition clears the interrupt adc_ready signal.	0
	R	ADC_INT_STAT	Returns the actual interrupt status of the adc_ready signal.	0
12	W	TSPX_INT_CLR	A '0' to '1' transition clears the interrupt of the TSPX signal.	0
	R	TSPX_INT_STAT	Returns the actual interrupt status of the TSPX signal.	0
13	W	TSMX_INT_CLR	A '0' to '1' transition clears the interrupt of the TSMX signal.	0
	R	TSMX_INT_STAT	Returns the actual interrupt status of the TSMX signal.	0

BIT	MODE	SYMBOL	REMARK	RESET
14	W	TCLIP_INT_CLR	A '0' to '1' transition clears the interrupt of the telecom clip.	0
	R	TCLIP_INT_STAT	Returns the actual interrupt status of the telecom clip.	0
15	W	ACLIP_INT_CLR	A '0' to '1' transition clears the interrupt of the audio clip.	0
	R	ACLIP_INT_STAT	Returns the actual interrupt status of the audio clip.	0
Address 5: Telecom control register A				
0 to 6	R/W	TEL_DIV[n]	Telecom codec sample rate divisor. Valid values lie between16 [0010000] and 127 [1111111].	16
7	R/W	TEL_LOOP	If '1', the voice band filter in the telecom input path is enabled.	0
Address 6: Telecom control register B				
3	R/W	TEL_VOICE_ENA	If '1', the voice band filter in the telecom input path is enabled.	0
4	R	TEL_CLIP_STAT	Returns the telecom clip detection status. (the telecom clip status will remain set until cleared by the user).	0
	W	TEL_CLIP_CLR	A '0' to '1' transition clears the telecom clip detection status.	0
6	R/W	TEL_ATT	If '1', the telecom input attenuation (6 dB) is enabled.	0
11	R/W	TEL_SIDE_ENA	If '1', the sidetone suppression circuit is activated.	0
13	R/W	TEL_MUTE	If '1', the telecom output is muted.	0
14	R/W	TEL_IN_ENA	If '1', the telecom input path is activated.	0
15	R/W	TEL_OUT_ENA	If '1', the telecom output path is activated.	0
Address 7: Audio control register A				
0 to 6	R/W	AUD_DIV[n]	Audio codec sample rate divisor. Valid values lie between 6 [0000110] and 127 [1111111].	6
7 to 11	R/W	AUD_GAIN[n]	Audio input gain setting. Values range from 0 dB [00000] to 22.5 dB [01111]	0
Address 8: Audio control register B				
0 to 4	R/W	AUD_ATT[n]	Audio output attenuation setting. Values range from 0 dB [00000] to 69 dB [11111].	0
6	R	AUD_CLIP_STAT	Returns the audio clip detection status. If '1', the audio clip detection circuit is activated (The audio clip status will remain set until it is cleared by the user)	0
	W	AUD_CLIP_CLR	If ‘0’ to ‘1’ transition clears the audio clip detection status.	0
8	R/W	AUD_LOOP	If '1', the loopback mode in the audio codec is activated.	0
13	R/W	AUD_MUTE	If '1', the audio output is muted.	0
14	R/W	AUD_IN_ENA	If'1, the audio codec input path is activated.	0
15	R/W	AUD_OUT_ENA	If '1', the audio codec output path is activated.	0
Address 9:Touch screen control register				
0	R/W	TSMX_POW	If ‘1’, the TSMX pin is powered.	0
1	R/W	TSPX_POW	If ‘1’, the TSPX pin is powered.	0
2	R/W	TSMY_POW	If ‘1’, the TSMY pin is powered.	0
3	R/W	TSPY_POW	If ‘1’, the TSPY pin is powered.	0
4	R/W	TSMX_GND	If ‘1’, the TSMX pin is grounded.	0

BIT	MODE	SYMBOL	REMARK	RESET
5	R/W	TSPX_GND	If ‘1’, the TSPX pin is grounded.	0
6	R/W	TSMY_GND	If ‘1’, the TSMY pin is grounded.	0
7	R/W	TSPY_GND	If ‘1’, the TSPY pin is grounded.	0
8 and 9	R/W	TSC_MODE[n]	Touch screen operation mode: 00: interrupt mode 01: pressure measurement mode 1x: position measurement mode.	0
11	R/W	TSC_BIAS_ENA	If ‘1’, the touch screen bias circuit is activated.	0
12	R	TSPX_LOW	This bit returns the inverted state of the TSPX pin, ‘0’ is a high voltage (pen up), ‘1’ is a low voltage (pen down).	0
13	R	TSMX_LOW	This bit returns the inverted state of the TSMX pin, ‘0’ is a high voltage (pen up), ‘1’ is a low voltage (pen down).	0
Address 10: ADC control register				
0	R/W	ADC_SYNC_ENA	If ‘1’, the ADC sync mode is activated.	
1	R/W	VREFBYP_CON	If ‘1’, the internal reference voltage is connected to VREFBYP (pin 16).	
2 to 4	R/W	ADC_INPUT[n]	ADC input select: 000: TSPX 100: AD0 001: TSMX 101: AD1 010: TSPY 110: AD2 011: TSMY 110: AD3	0
5	R/W	EXT_REF_ENA	If ‘1’, an external reference voltage has to be applied to VREFBYP.	0
7	R/W	ADC_START	A ‘0’ to ‘1’ transition starts the ADC conversion sequence.	0
15	R/W	ADC_ENA	If ‘1’, the ADC circuit is activated.	0
Address 11: ADC data register				
5 to 14	R	ADC_DATA[n]	Returns the ADC result	0
15	R	ADC_DAT_VAL	Returns '0' if an ADC conversion is in progress. Returns '1' if the ADC conversion is completed and the ADC data is stored in the ADC_DATA[n] register.	0
Address 12: ID register				
0 to 5	R	VERSION[n]	Returns 000011 for all the UCB1100 circuits meeting this specification	0
6 to 11	R	DEVICE[n]	Returns 000000 for all the UCB1100 circuits meeting this specification	0
12 to 15	R	SUPPLIER[n]	Returns 0001 for all the UCB1100 circuits meeting this specification	0
Address 13: MODE register; note 1				
0	R/W	AUD_TEST	If ‘1’, the analog audio test mode is activated.(2)	0
1	R/W	TEL_TEST	If ‘1’, the analog telecom test mode is activated.(2)	0
2 to 5	R/W	PROD_TEST_MODE	These bits select the built-in production test modes.(2)	0

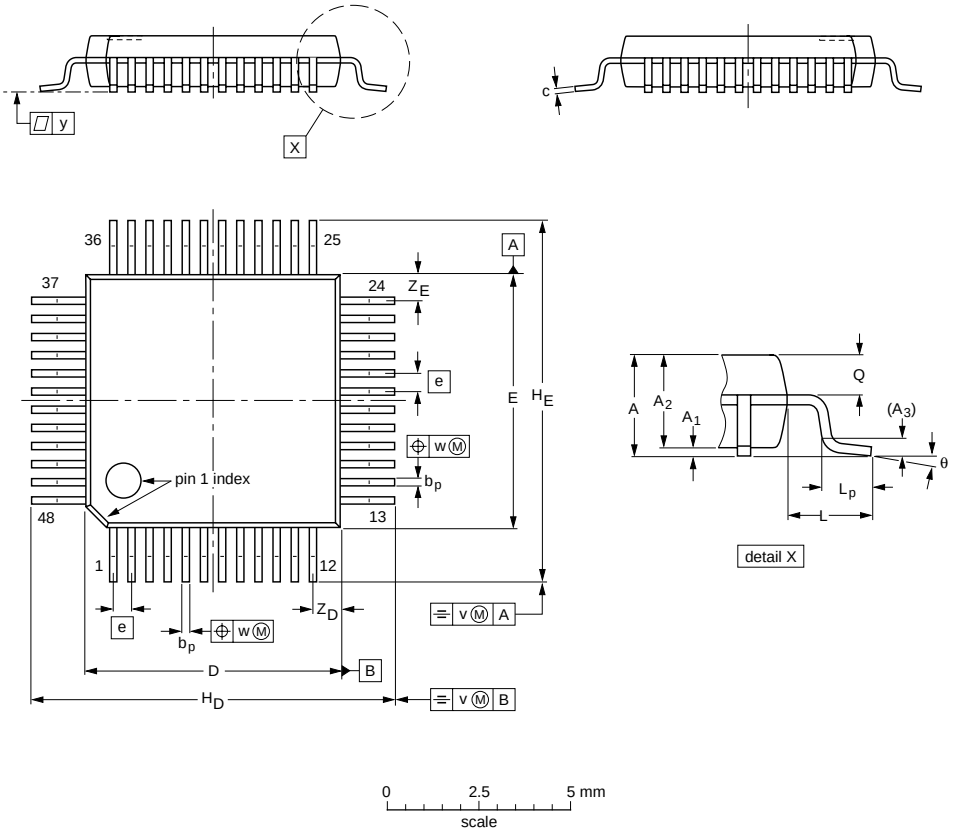
BIT	MODE	SYMBOL	REMARK	RESET
12	R/W	DYN_VFLAG_ENA	If ‘1’, the dynamic data valid flag mode is activated for both the audio and the telecom data valid flag.	0
13	R/W	AUD_OFF_CAN	If ‘1’, the offset cancelling circuit in the audio input path is enabled.	0
14	R/W		Reserved, should be ‘0’	0
15	R/W		Reserved, should be ‘0’	0
Address 14: Reserved				
			Reserved for future use.	
Address 15: NULL register				
0 to 15	R		Returns [1111111111111111] at all times	

Note

1. Activating one or more test modes changes the functionality of the UCB1100.
2. TEST (pin 13) must be HIGH when writing to these bits.

PACKAGE OUTLINES

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~93-06-15~~ 94-12-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.